FIG. 1

FIRST TECHNIQUE

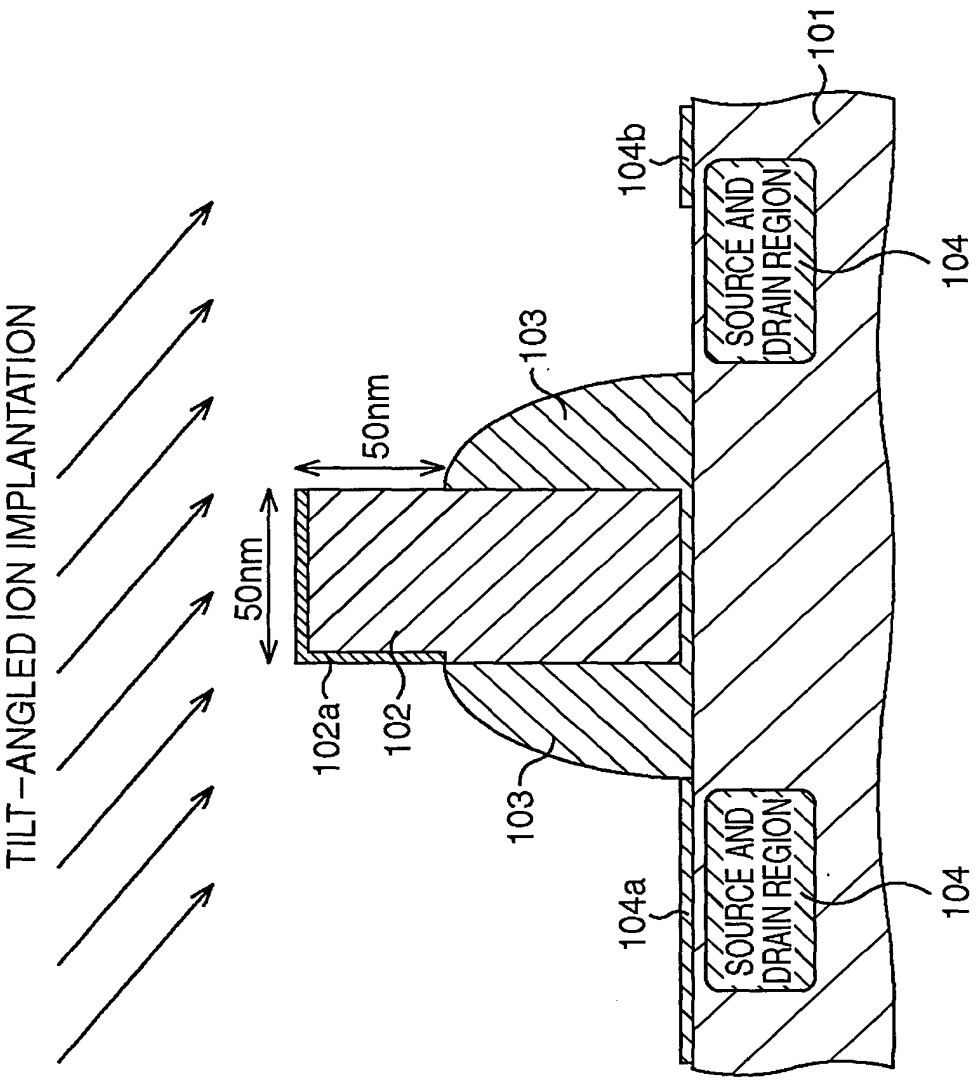


FIG. 2

SECOND TECHNIQUE

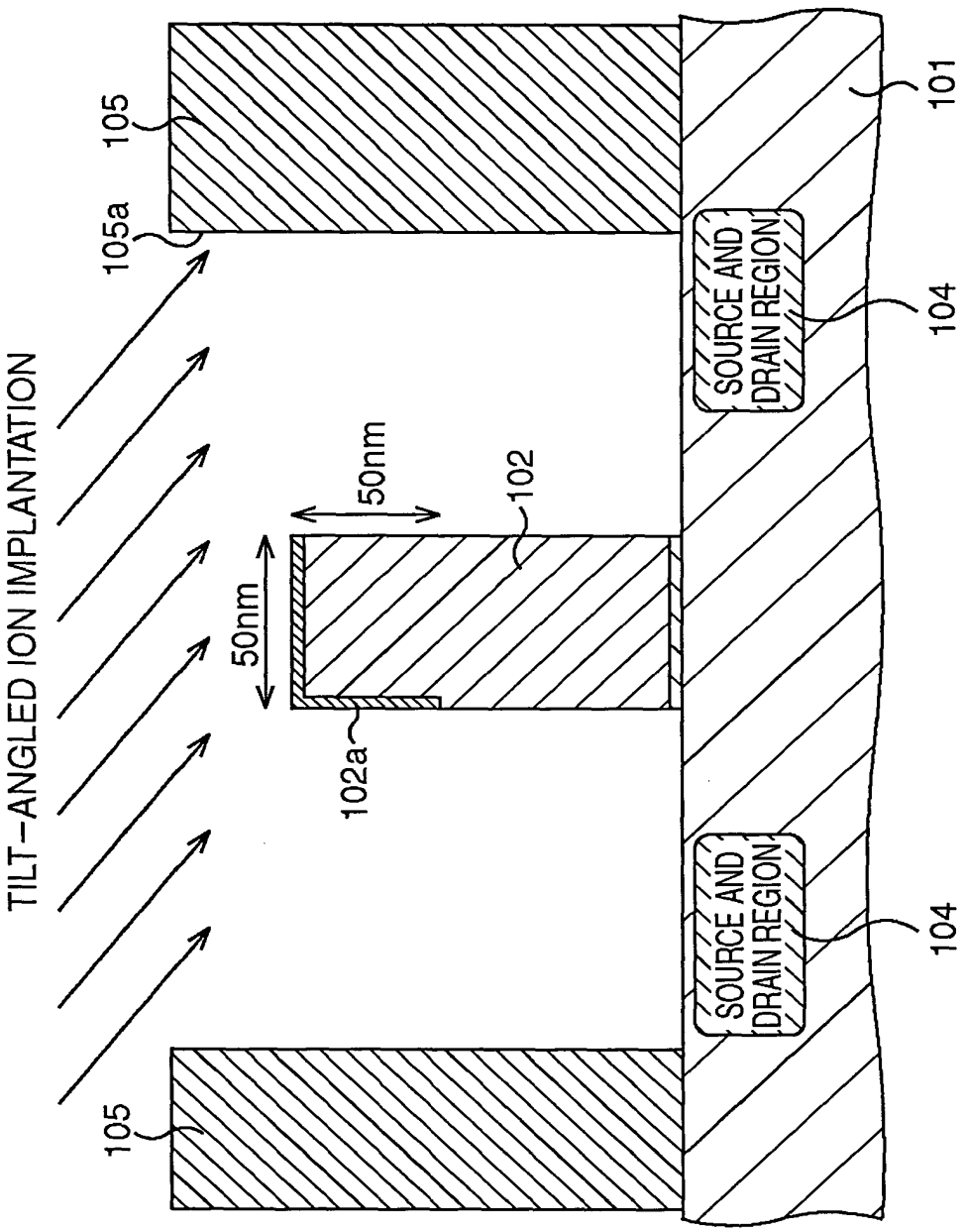


FIG. 3

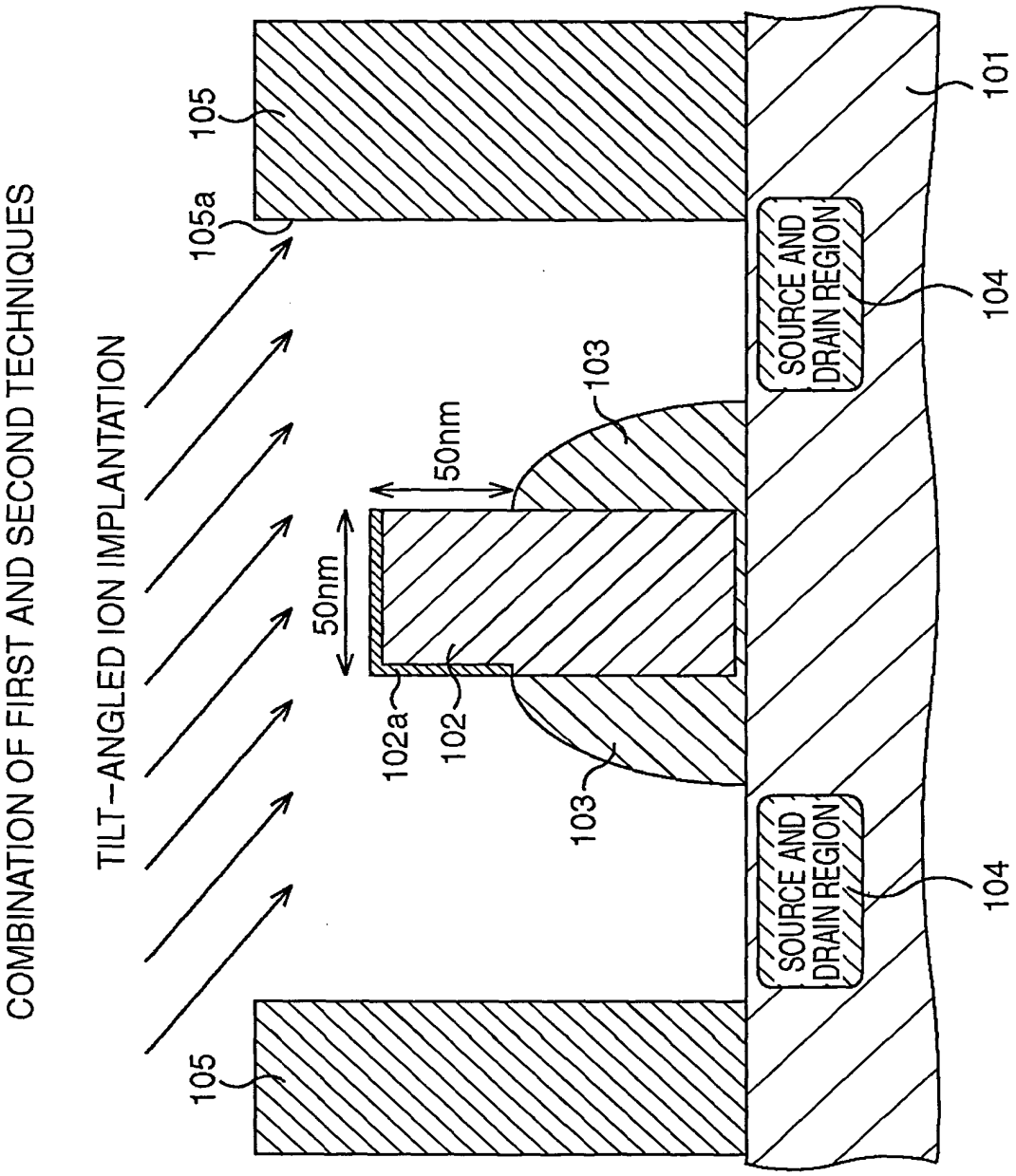
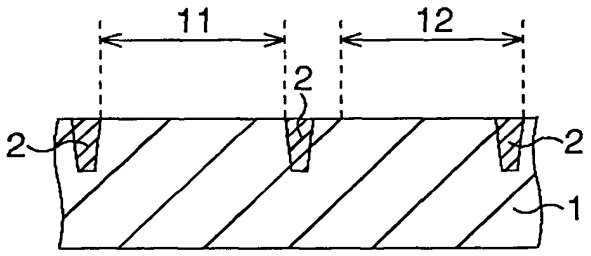
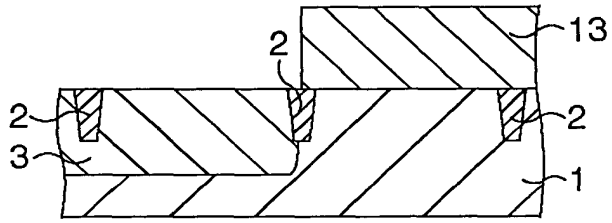

COMBINATION OF FIRST AND SECOND TECHNIQUES
TILT-ANGLED ION IMPLANTATION
105
105a
101
SOURCE AND DRAIN REGION
104
103
50nm
50nm
102a
102
103
SOURCE AND DRAIN REGION
104
105

FIG. 4A



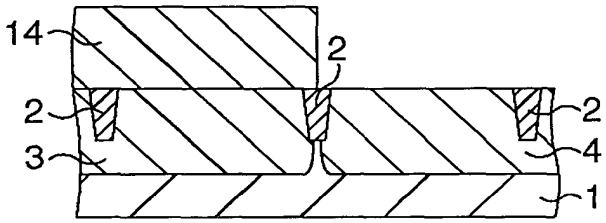
STI FORMATION

FIG. 4B



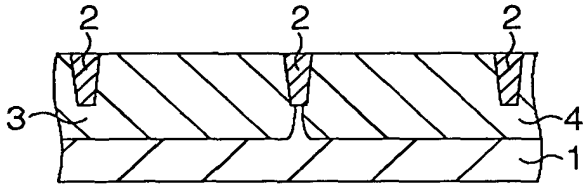
nMOS WELL FORMATION, CHANNEL IMPLANTATION

FIG. 4C



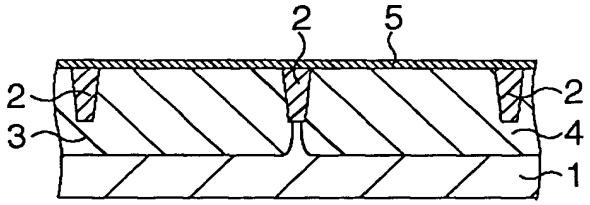
pMOS WELL FORMATION, CHANNEL IMPLANTATION

FIG. 4D



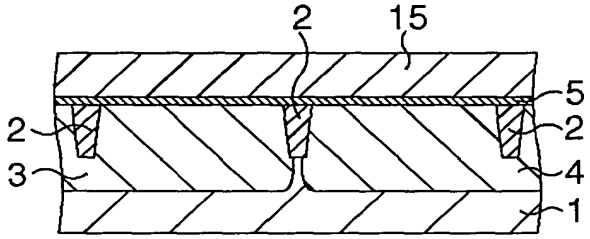
ANNEALING (RTA, 1,000°C, 3 sec)

FIG. 5A



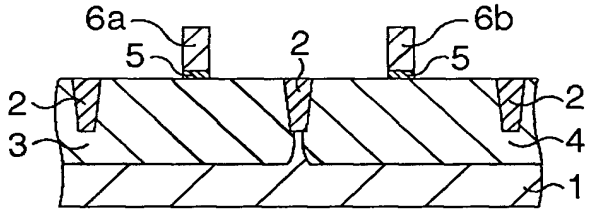
GATE OXIDATION

FIG. 5B



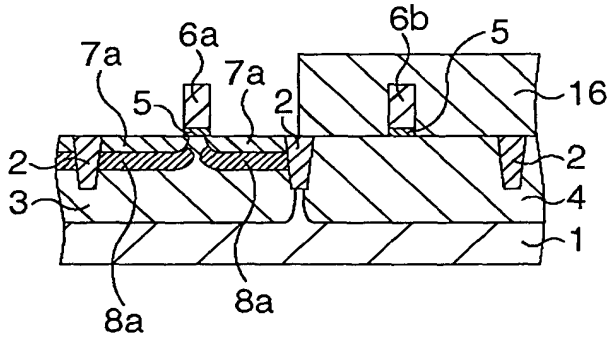
POLYSILICON DEPOSITION

FIG. 5C



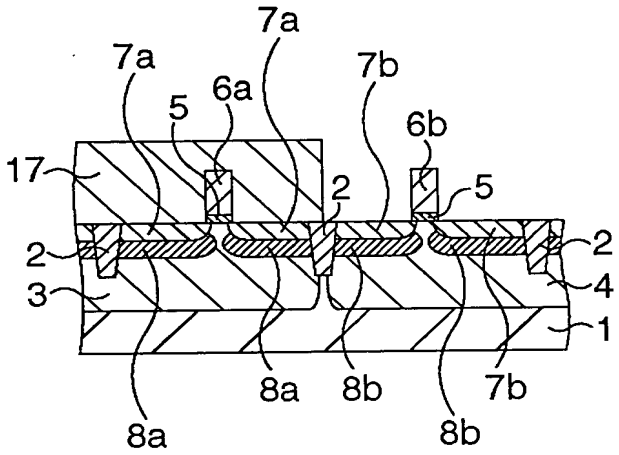
POLYSILICON ETCHING

FIG. 5D



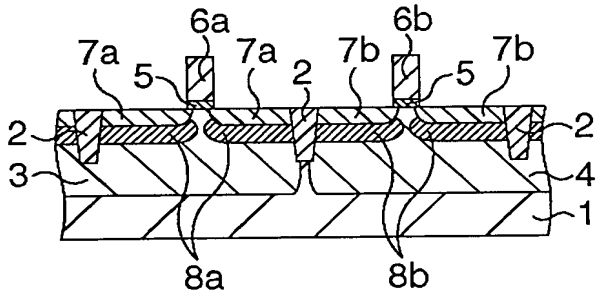
nMOS EXTENSION AND POCKET IMPLANTATIONS

FIG. 6A



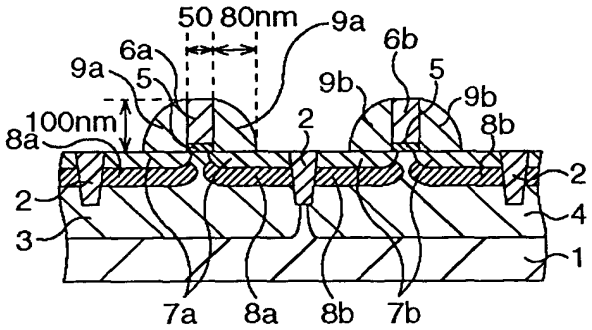
PMOS EXTENSION AND POCKET IMPLANTATIONS

FIG. 6B



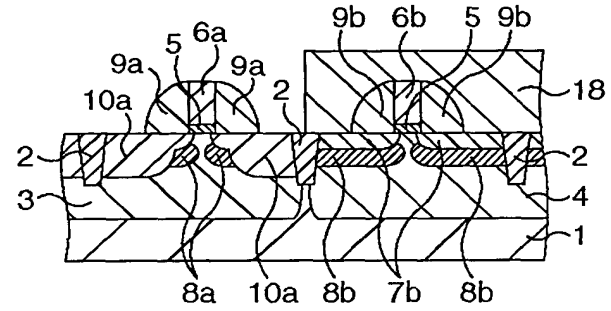
ANNEALING (RTA, 1,000°C, 1 sec)

FIG. 7A



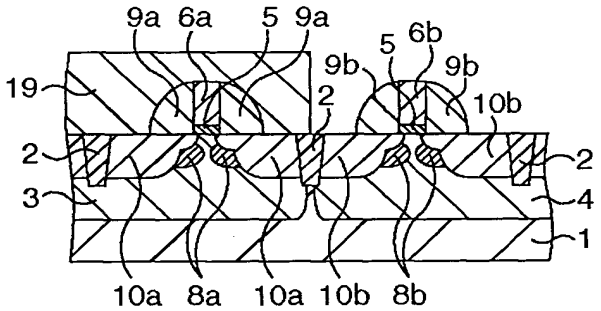
SIDEWALL FORMATION

FIG. 7B



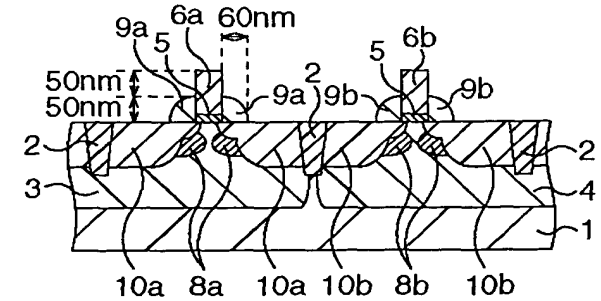
nMOS S/D ION IMPLANTATION (P, 8 keV, 4.5×10^{15}, 0°)

FIG. 7C



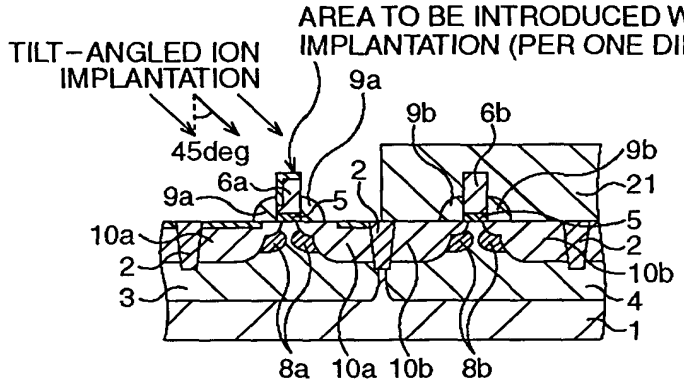
pMOS S/D ION IMPLANTATION (B, 4 keV, 2.25×10^{15}, 0°)

FIG. 7D



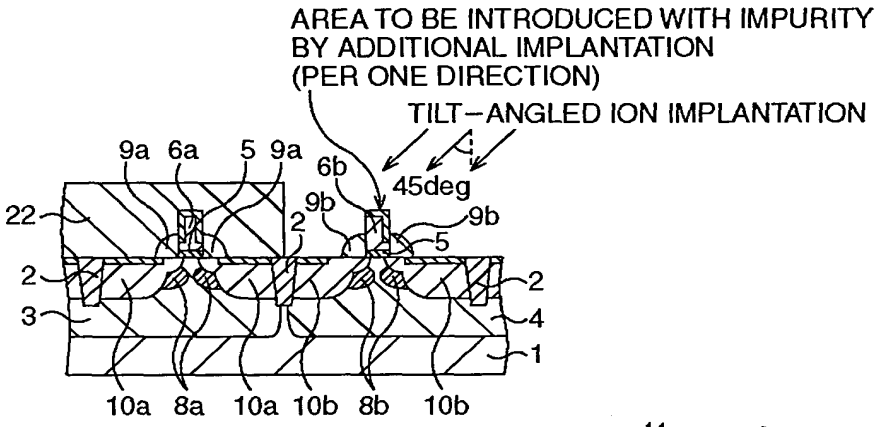
SIDEWALL THINNING (DRY ETCHING, THINNED BY 50 nm)

FIG. 8A



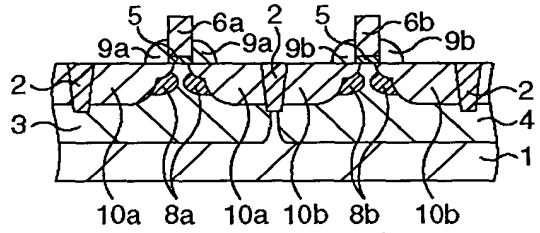
ADDITIONAL IMPLANTATION FOR nMOS GATE (P, 4 keV, $5 \times 10^{14} \times 4$, 45°)

FIG. 8B



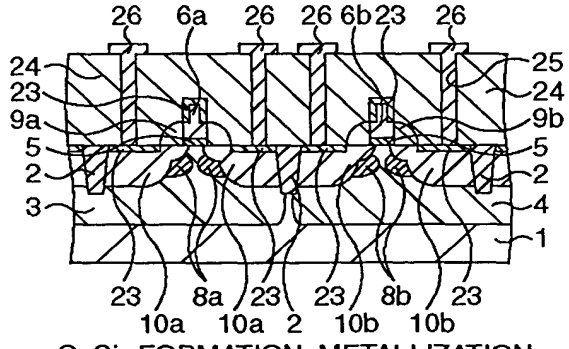
ADDITIONAL IMPLANTATION FOR pMOS GATE (B, 2 keV, $2.5 \times 10^{14} \times 4$, 45°)

FIG. 8C



ANNEALING (RTA, 1,030°C, 1 sec)

FIG. 8D



$CoSi_2$ FORMATION, METALLIZATION

FIG. 9

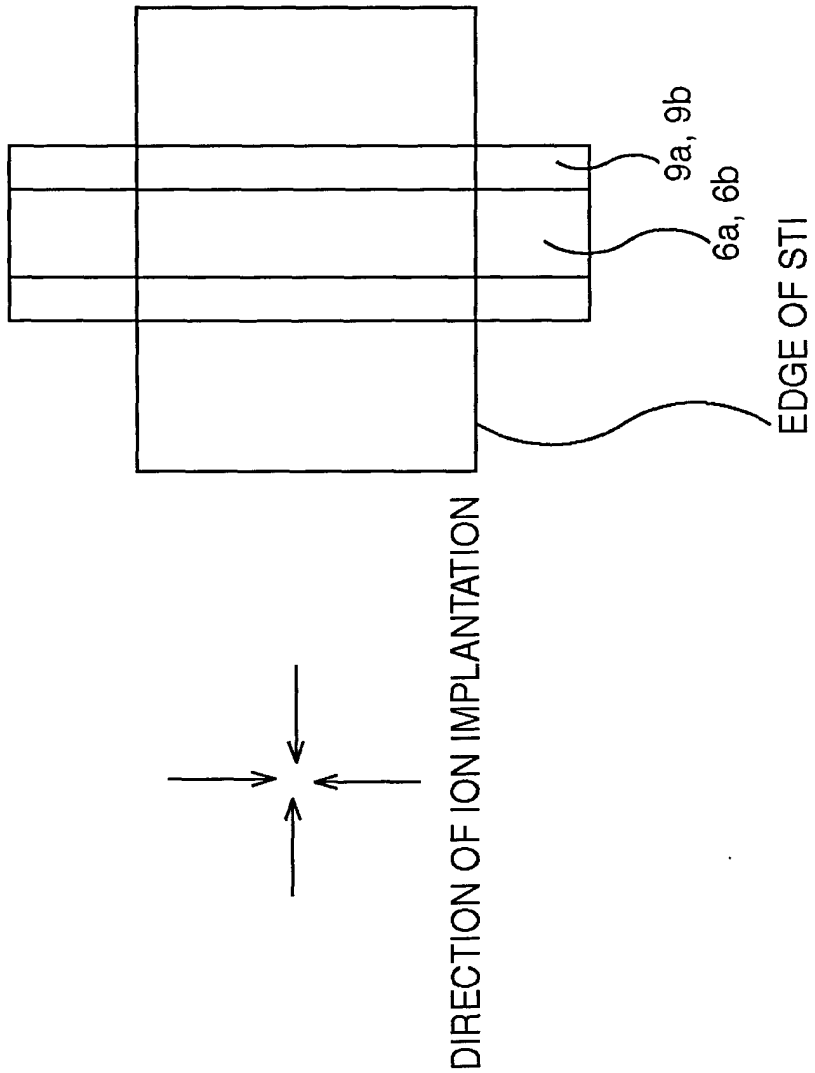


FIG. 10

MODIFIED EXAMPLE OF FIRST EMBODIMENT

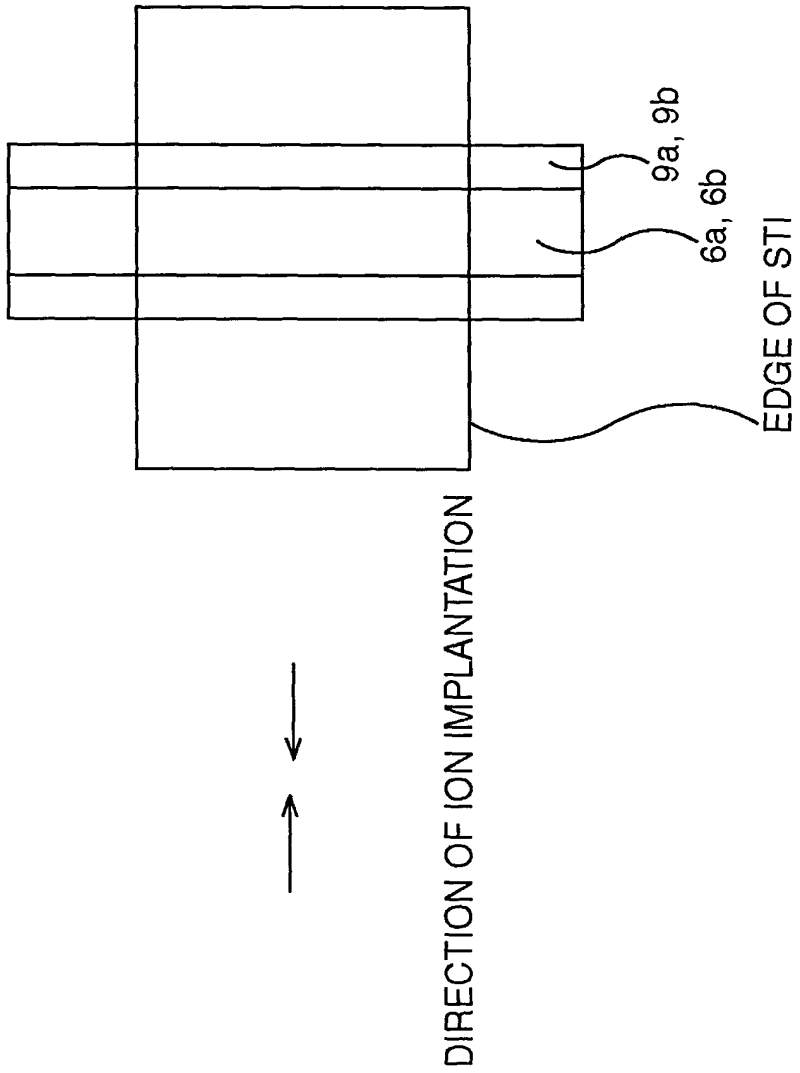
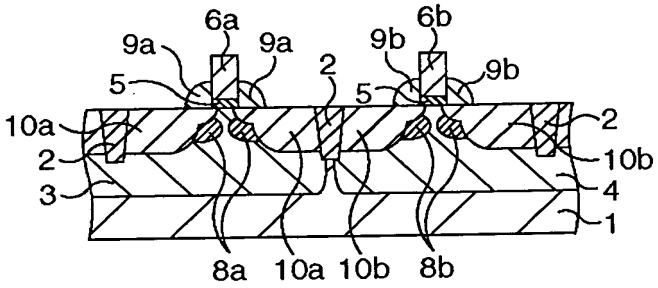


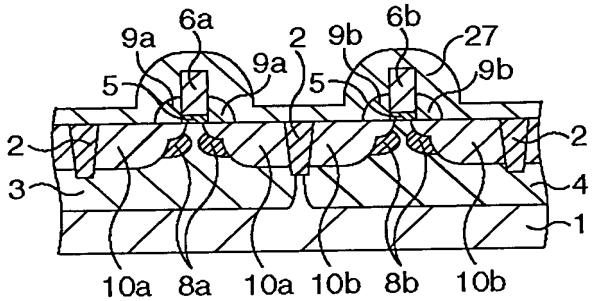
FIG. 11A

PROCESS STEPS BEFORE ANNEALING ARE SAME AS THOSE IN THE FIRST EMBODIMENT SHOWN IN FIG. 8B



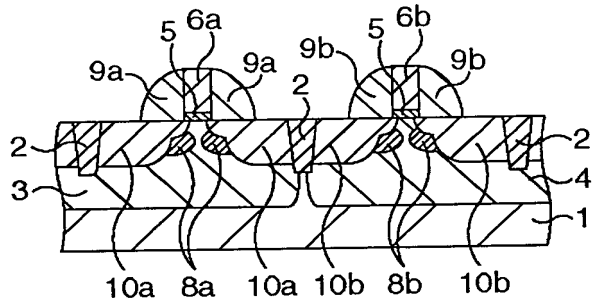
ANNEALING (RTA, 1,030°C, 1 sec)

FIG. 11B



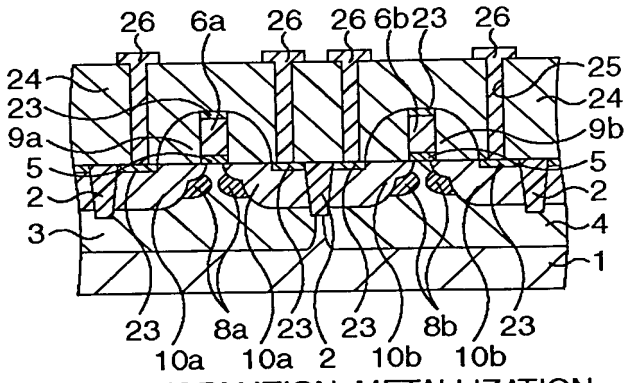
OXIDE FILM DEPOSITION

FIG. 11C



OXIDE FILM ETCH-BACK

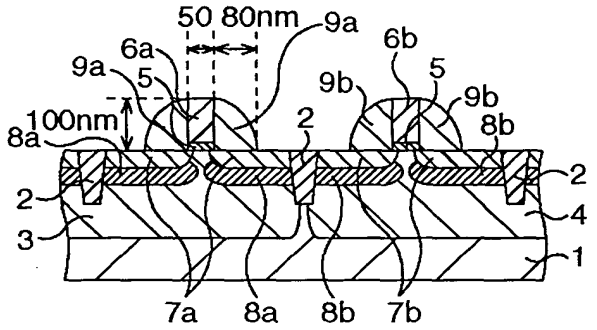
FIG. 11D



$CoSi_2$ FORMATION, METALLIZATION

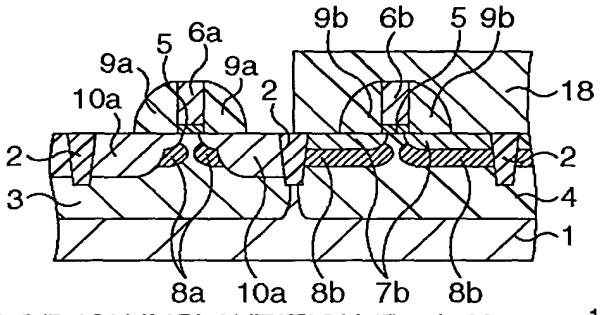
FIG. 12A

PROCESS STEPS BEFORE SIDEWALL FORMATION ARE SAME AS THOSE IN THE FIRST EMBODIMENT SHOWN IN FIG. 6B



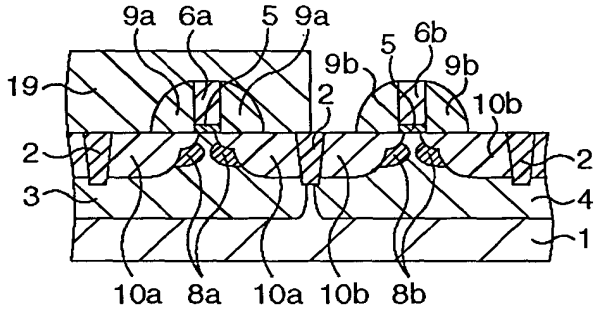
SIDEWALL FORMATION

FIG. 12B



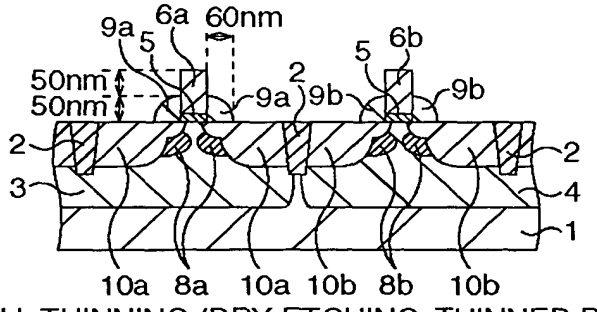
nMOS S/D ION IMPLANTATION (P, 8 keV, 5×10^{15}, 0°)

FIG. 12C



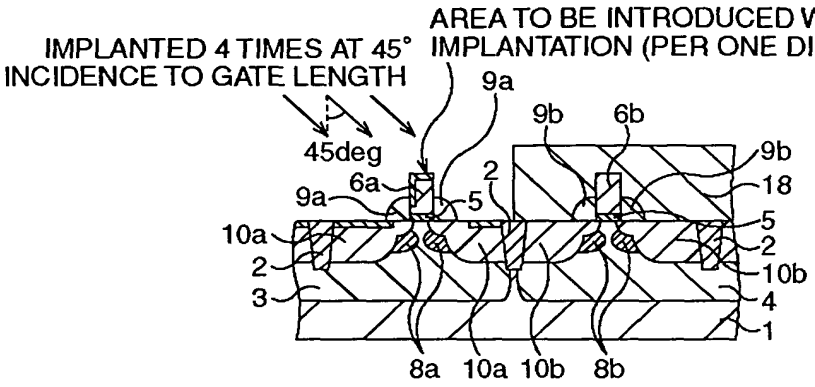
pMOS S/D ION IMPLANTATION (B, 4 keV, 2.5×10^{15}, 0°)

FIG. 12D



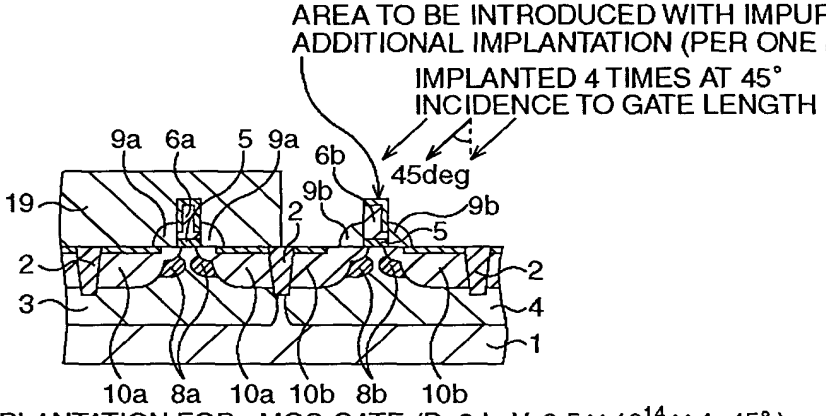
SIDEWALL THINNING (DRY ETCHING, THINNED BY 50 nm)

FIG. 13A



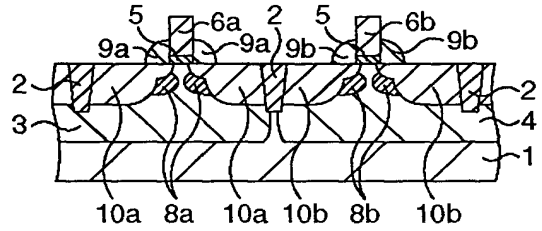
ADDITIONAL IMPLANTATION FOR nMOS GATE (P, 4 keV, $5 \times 10^{14} \times 4$, 45°)

FIG. 13B



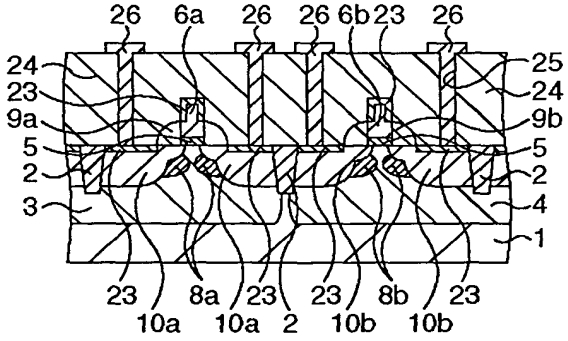
ADDITIONAL IMPLANTATION FOR pMOS GATE (B, 2 keV, $2.5 \times 10^{14} \times 4$, 45°)

FIG. 13C



ANNEALING (RTA, 1,030°C, 1 sec)

FIG. 13D



$CoSi_2$ FORMATION, METALLIZATION

FIG. 14

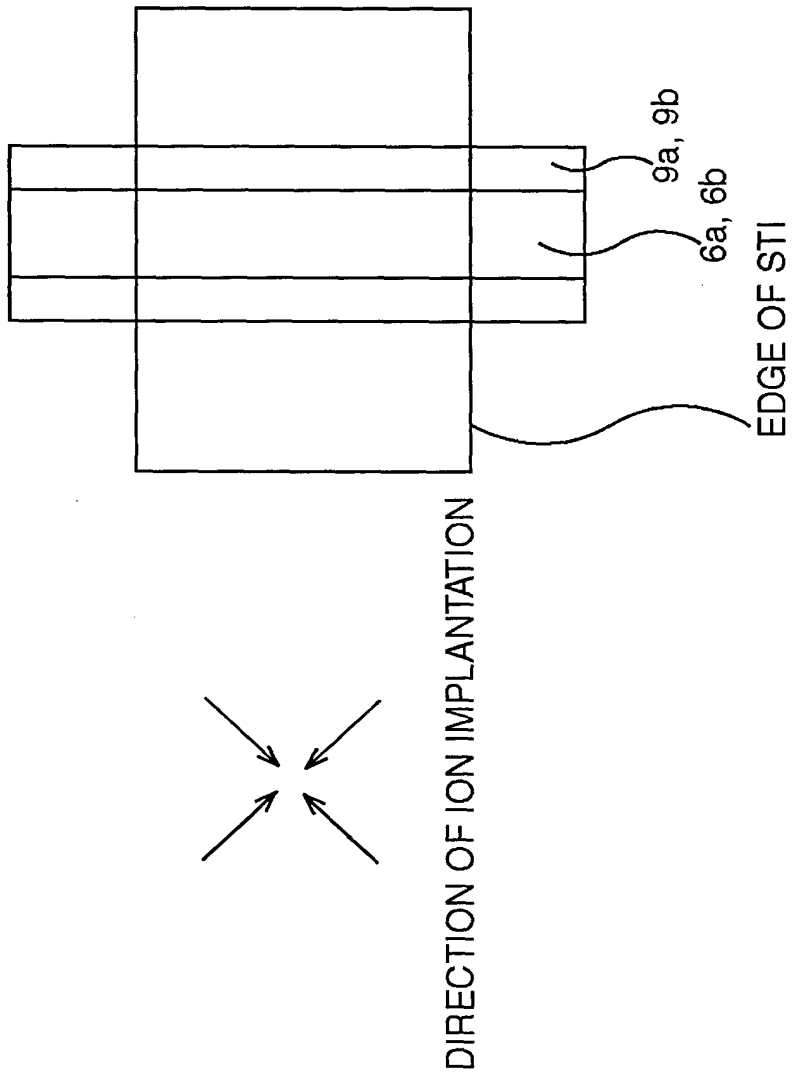
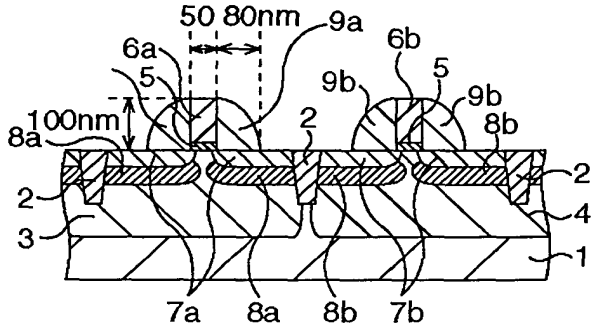


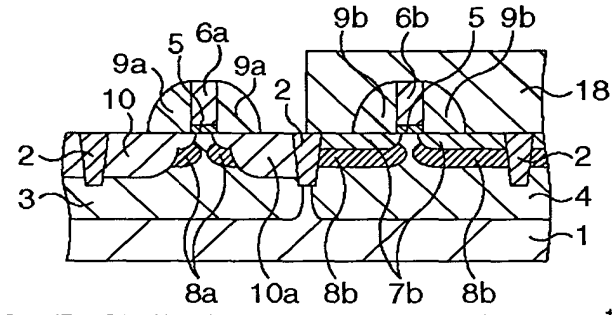
FIG. 15A

PROCESS STEPS BEFORE SIDEWALL FORMATION ARE SAME AS THOSE IN THE FIRST EMBODIMENT SHOWN IN FIG. 6B



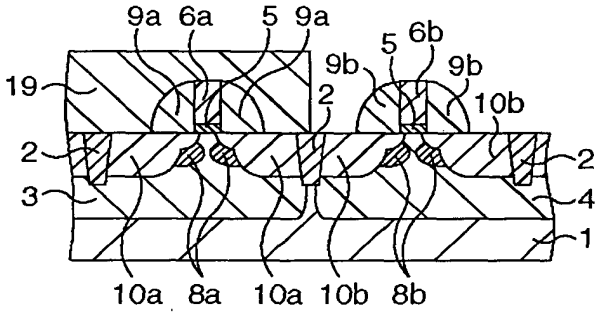
SIDEWALL FORMATION

FIG. 15B



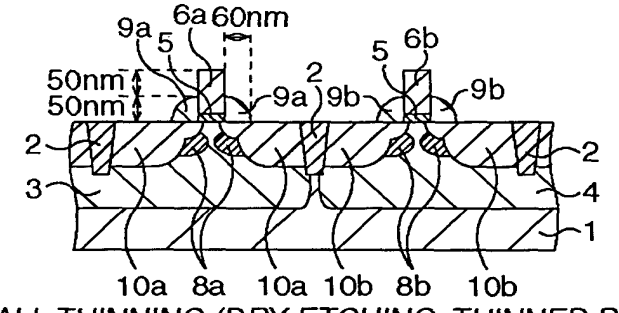
nMOS S/D ION IMPLANTATION (P, 8 keV, 5×10^{15}, 0°)

FIG. 15C



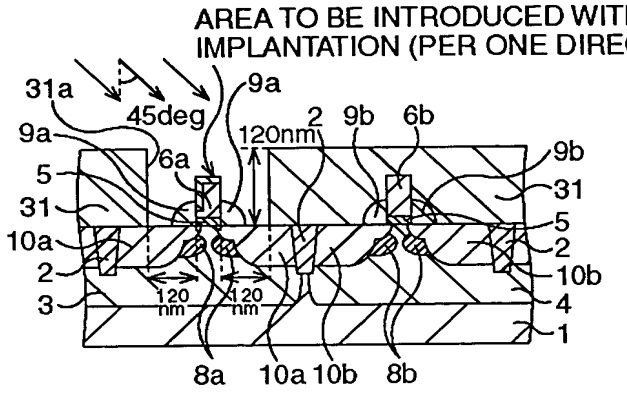
pMOS S/D ION IMPLANTATION (B, 4 keV, 2.5×10^{15}, 0°)

FIG. 15D



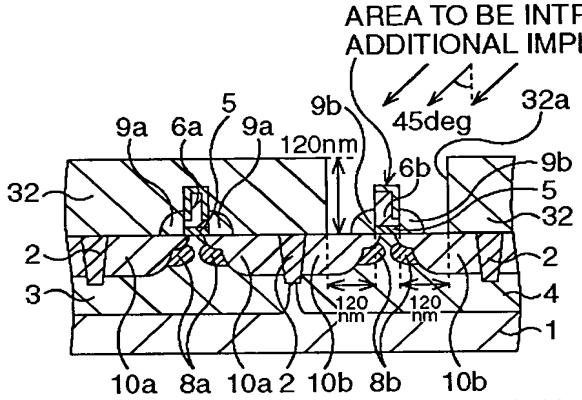
SIDEWALL THINNING (DRY ETCHING, THINNED BY 50 nm)

FIG. 16A



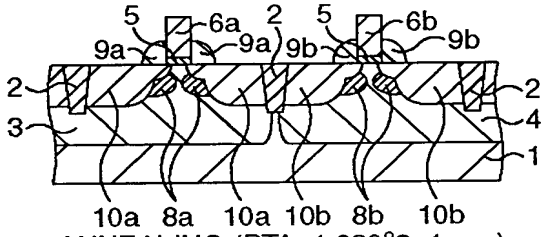
ADDITIONAL IMPLANTATION FOR nMOS GATE (P, 4 keV, $5 \times 10^{14} \times 4$, 45°)

FIG. 16B



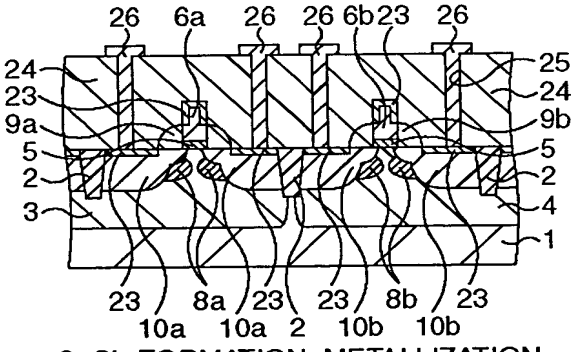
ADDITIONAL IMPLANTATION FOR pMOS GATE (B, 2 keV, $2.5 \times 10^{14} \times 4$, 45°)

FIG. 16C



ANNEALING (RTA, 1,030°C, 1 sec)

FIG. 16D



$CoSi_2$ FORMATION, METALLIZATION

FIG. 17

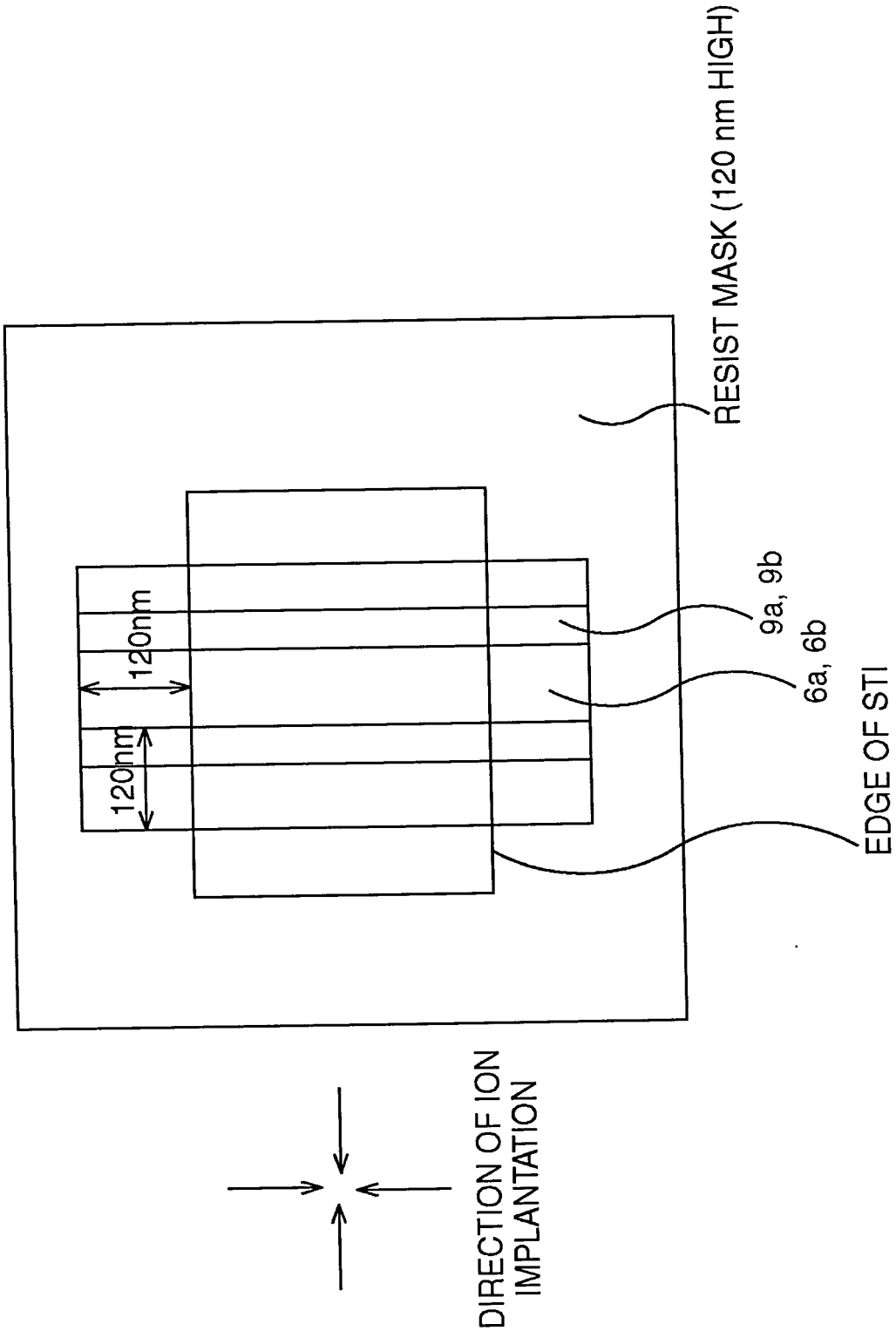
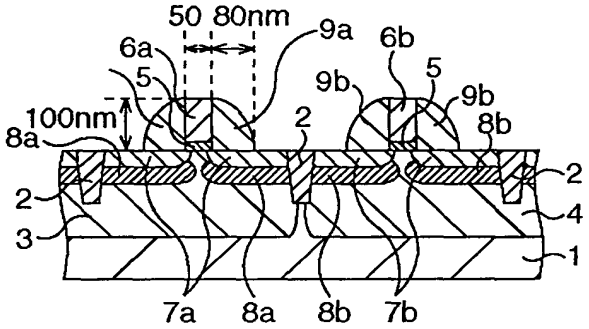

RESIST MASK (120 nm HIGH)
9a, 9b
6a, 6b
EDGE OF STI
120nm
120nm
DIRECTION OF ION IMPLANTATION

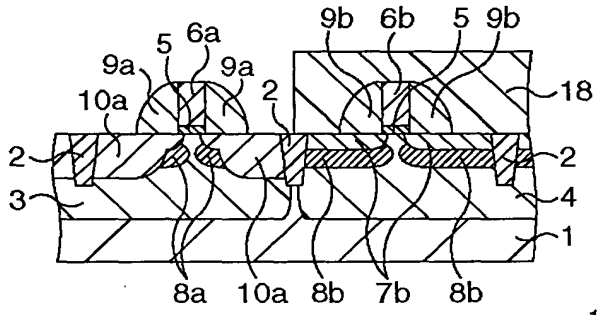
FIG. 18A

PROCESS STEPS BEFORE pMOS S/D ION IMPLANTATION ARE SAME AS THOSE IN THE FIRST EMBODIMENT SHOWN IN FIG. 6B



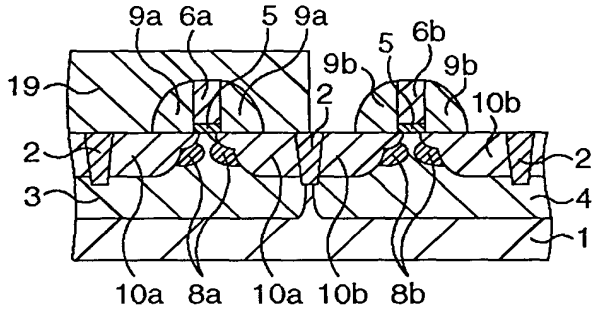
SIDEWALL FORMATION

FIG. 18B



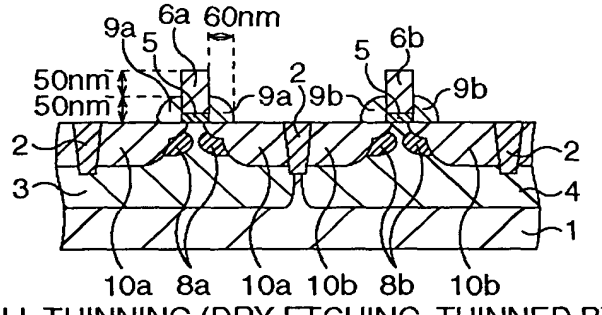
nMOS S/D ION IMPLANTATION (P, 8 keV, 6×10^{15}, 0°)

FIG. 18C



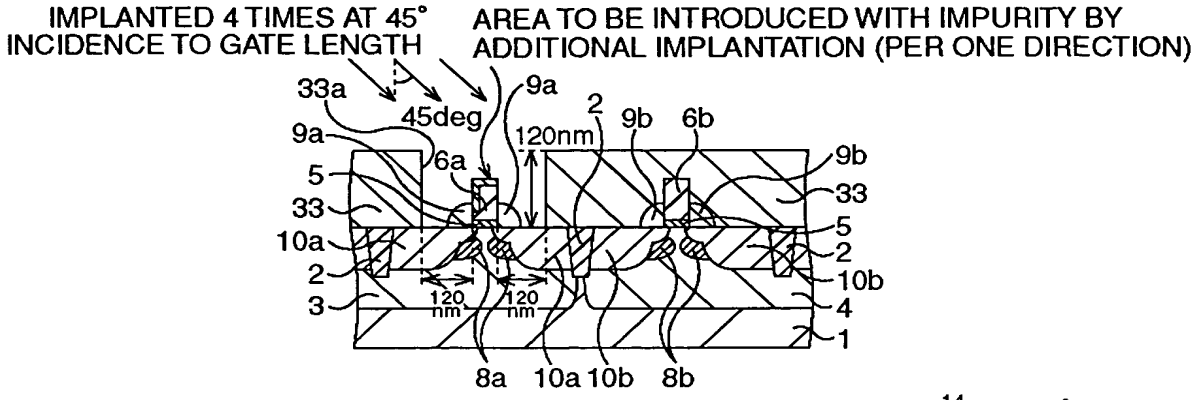
pMOS S/D ION IMPLANTATION (B, 4 keV, 3×10^{15}, 0°)

FIG. 18D



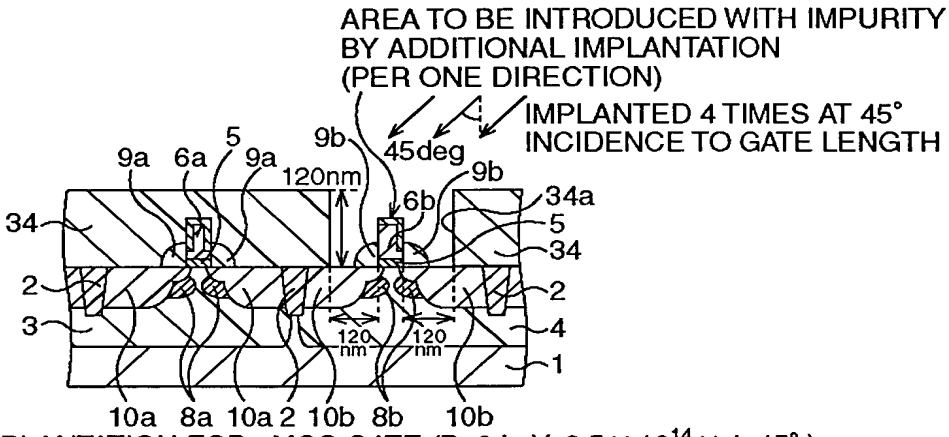
SIDEWALL THINNING (DRY ETCHING, THINNED BY 50 nm)

FIG. 19A



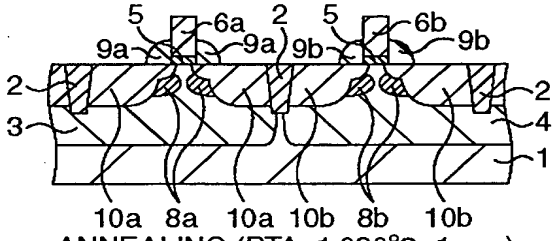
ADDITIONAL IMPLANTATION FOR nMOS GATE (P, 4 keV, $5 \times 10^{14} \times 4$, 45°)

FIG. 19B



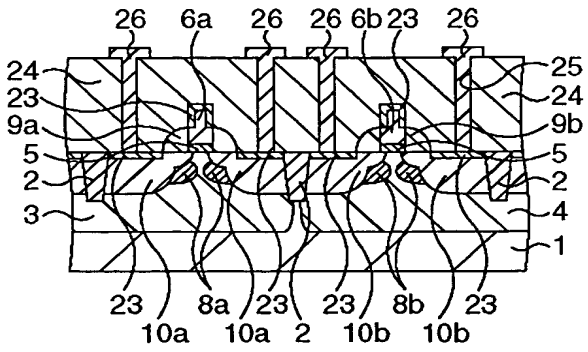
ADDITIONAL IMPLANTATION FOR pMOS GATE (B, 2 keV, $2.5 \times 10^{14} \times 4$, 45°)

FIG. 19C



ANNEALING (RTA, 1,030°C, 1 sec)

FIG. 19D



$CoSi_2$ FORMATION, METALLIZATION

FIG. 20

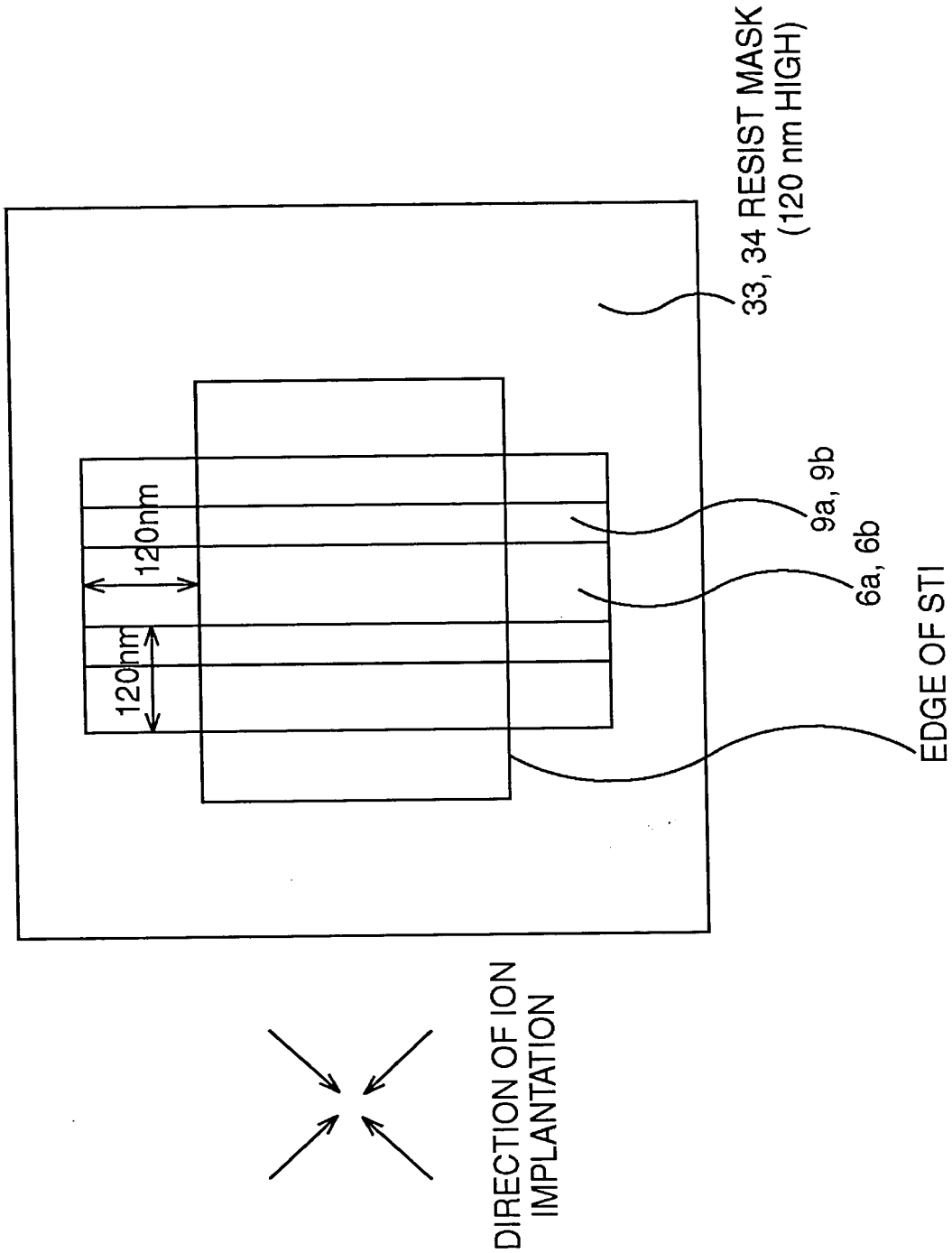
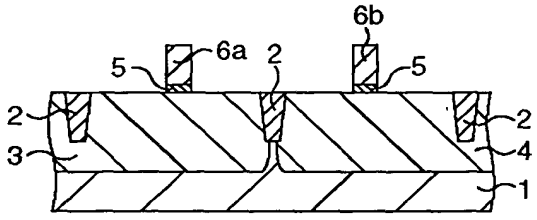

33, 34 RESIST MASK
(120 nm HIGH)
9a, 9b
6a, 6b
EDGE OF STI
120nm
120nm
DIRECTION OF ION
IMPLANTATION

FIG. 21A

PROCESS STEPS BEFORE PLYSILICON ETCHING ARE SAME AS THOSE IN THE FIRST EMBODIMENT SHOWN IN FIG.5C

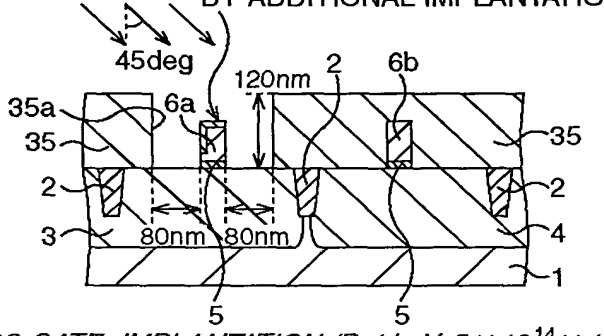


POLYSILICON ETCHING

FIG. 21B

IMPLANTED 4 TIMES AT 45° INCIDENCE TO GATE LENGTH

AREA TO BE INTRODUCED WITH IMPURITY BY ADDITIONAL IMPLANTATION (PER ONE DIRECTION)

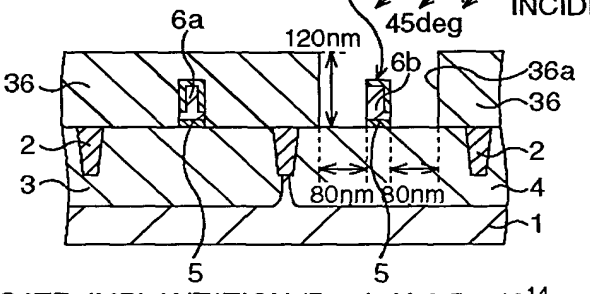


nMOS GATE IMPLANTATION (P, 4 keV, $5 \times 10^{14} \times 4$, 45°)

FIG. 21C

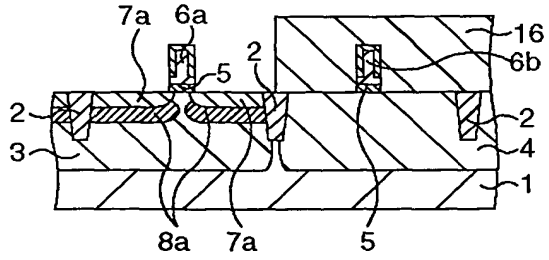
AREA TO BE INTRODUCED WITH IMPURITY BY ADDITIONAL IMPLANTATION (PER ONE DIRECTION)

IMPLANTED 4 TIMES AT 45° INCIDENCE TO GATE LENGTH



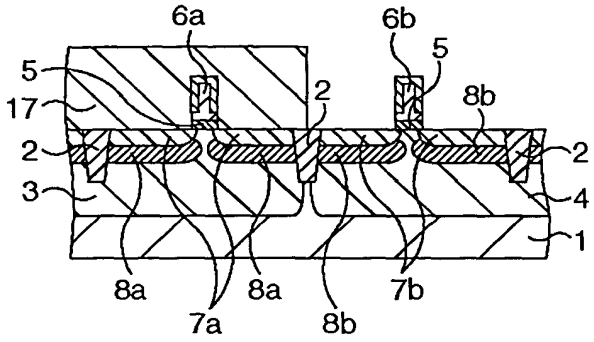
pMOS GATE IMPLANTATION (B, 2 keV, $2.5 \times 10^{14} \times 4$, 45°)

FIG. 21D



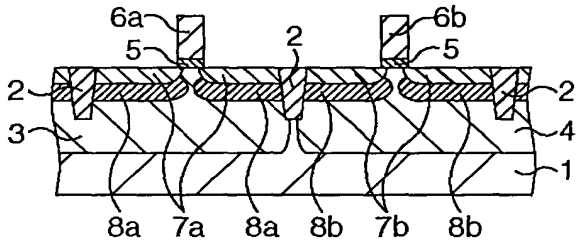
nMOS EXTENSION AND POCKET ION IMPLANTATION

FIG. 22A



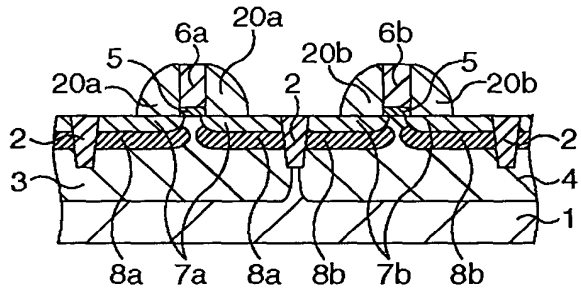
pMOS EXTENSION AND POCKET ION IMPLANTATION

FIG. 22B



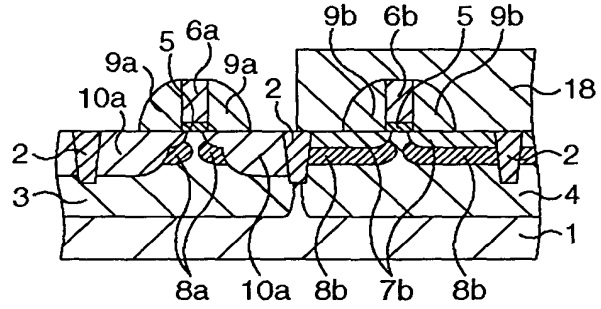
ANNEALING (RTA, 1,000°C, 1 sec)

FIG. 22C



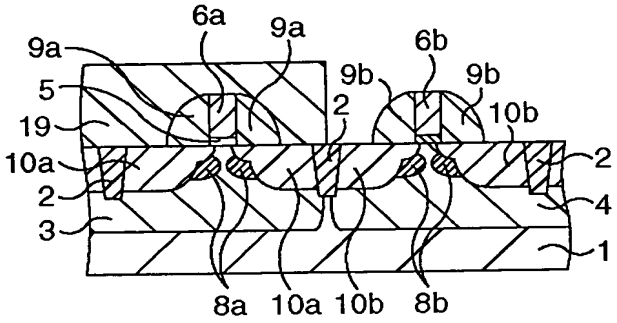
SIDEWALL FORMATION

FIG. 22D



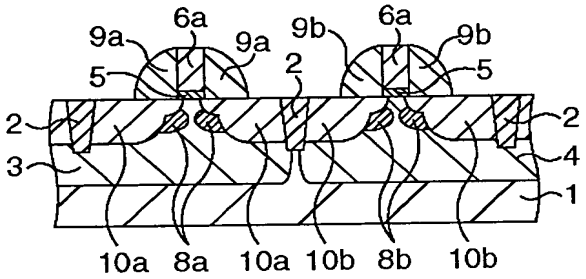
nMOS S/D ION IMPLANTATION (P, 8 keV, 6×10^{15}, 0°)

FIG. 23A



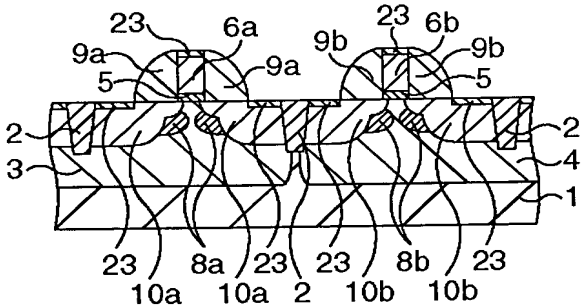
pMOS S/D ION IMPLANTATION (B, 4keV, 3×10^{15}, 0°)

FIG. 23B



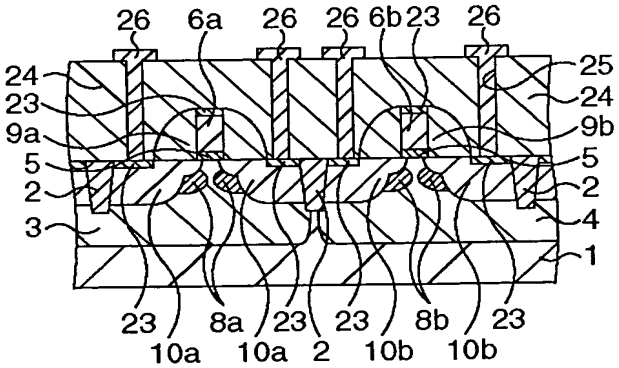
ANNEALING (RTA, 1,030°C, 1 sec)

FIG. 23C



$CoSi_2$ FORMATION

FIG. 23D



METALLIZATION

FIG. 24

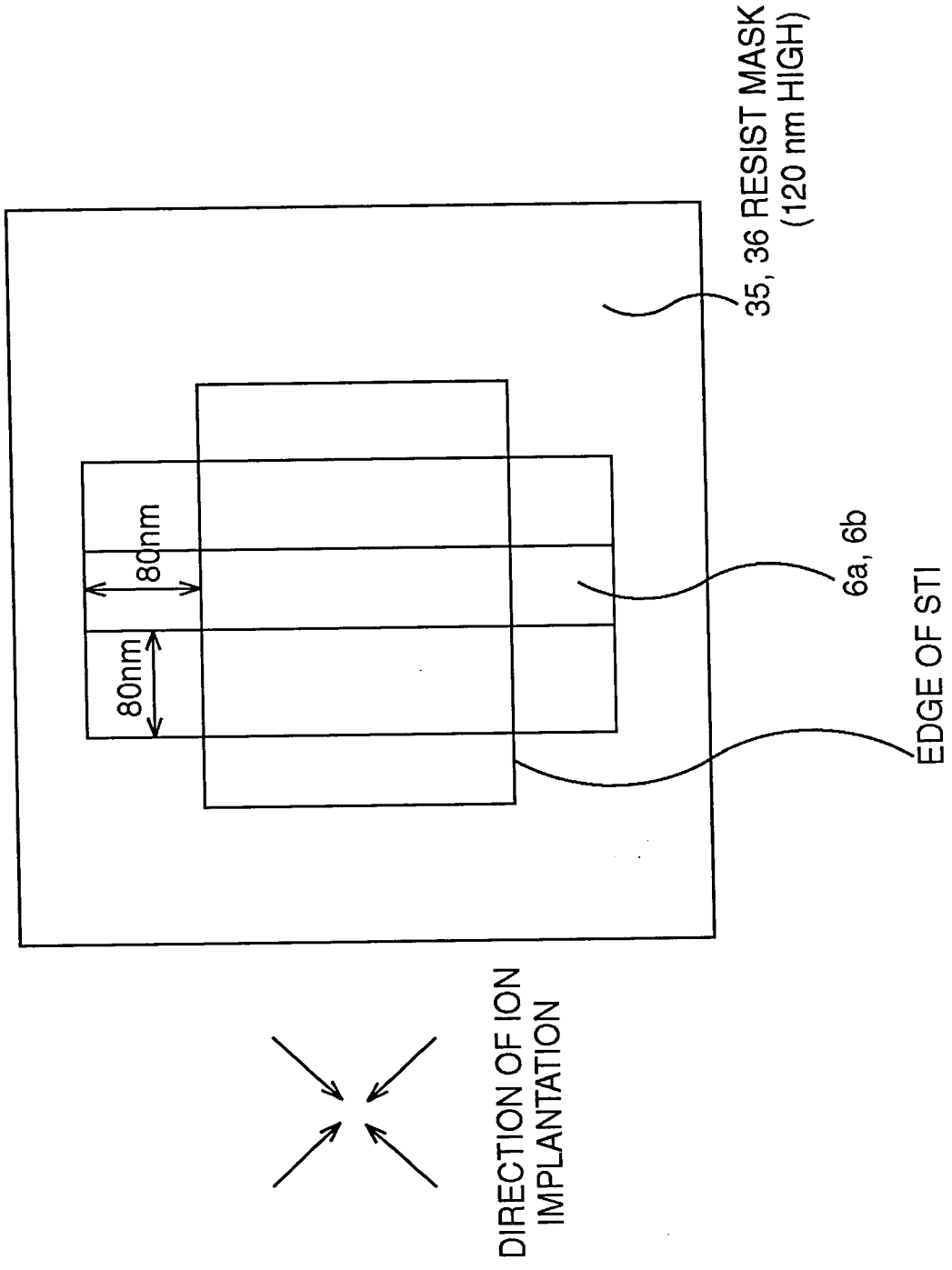
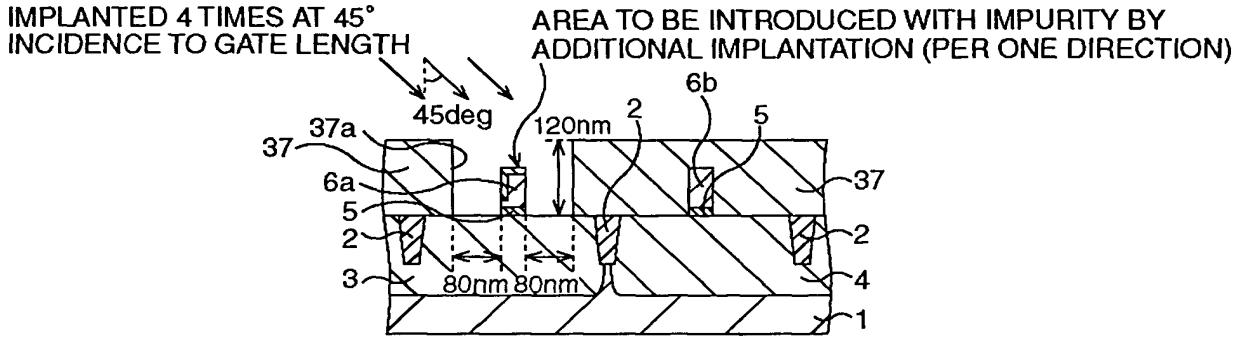

35, 36 RESIST MASK
(120 nm HIGH)
80nm
80nm
6a, 6b
EDGE OF STI
DIRECTION OF ION
IMPLANTATION

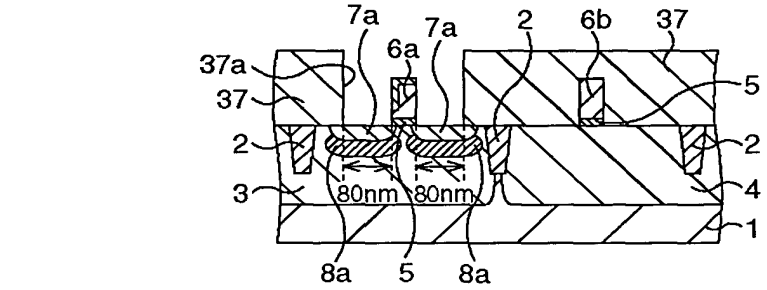
FIG. 25A

PROCESS STEPS BEFORE PLYSILICON ETCHING ARE SAME AS THOSE IN THE FIRST EMBODIMENT SHOWN IN FIG.5C



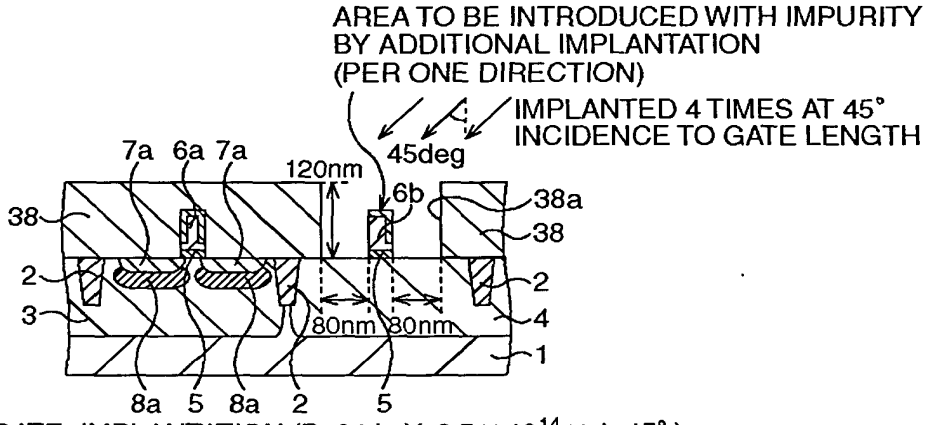
nMOS GATE IMPLANTATION (P, 4 keV, $5 \times 10^{14} \times 4$, 45°)

FIG. 25B



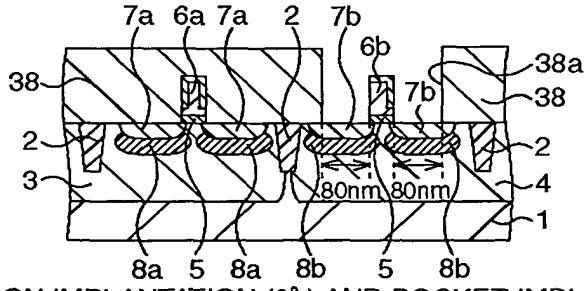
nMOS EXTENSION IMPLANTATION (0°) AND POCKET IMPLANTATION (15°)

FIG. 25C



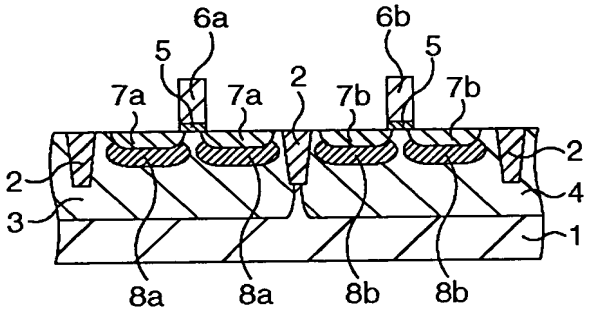
pMOS GATE IMPLANTATION (B, 24 keV, $2.5 \times 10^{14} \times 4$, 45°)

FIG. 25D



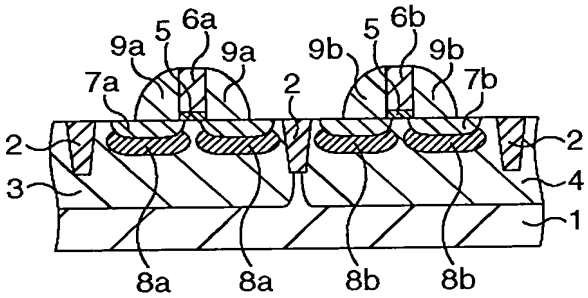
pMOS EXTENSION IMPLANTATION (0°) AND POCKET IMPLANTATION (15°)

FIG. 26A



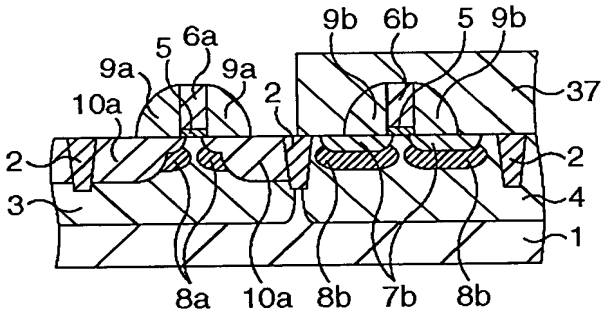
ANNEALING (RTA, 1,000°C, 1 sec)

FIG. 26B



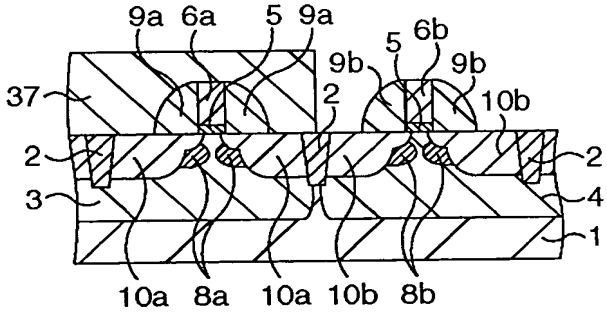
SIDEWALL FORMATION

FIG. 26C



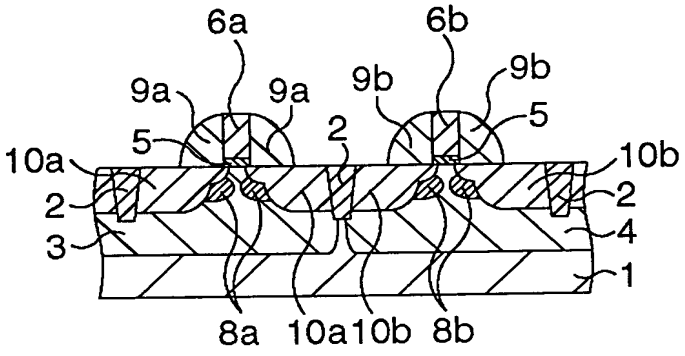
nMOS S/D ION IMPLANTATION (P, 8keV, 6.0×10^{15}, 0°)

FIG. 26D



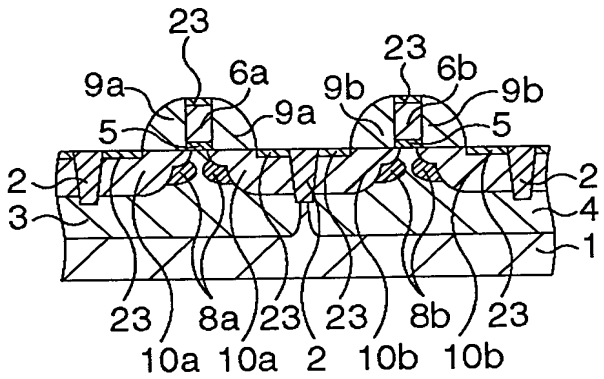
pMOS S/D ION IMPLANTATION (B, 4keV, 3×10^{15}, 0°)

FIG. 27A



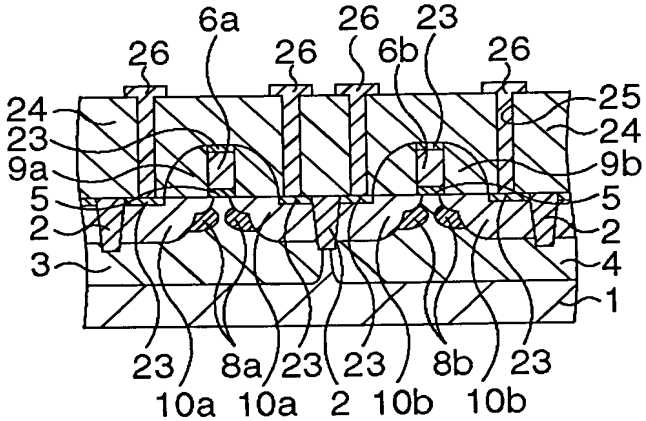
ANNEALING (RTA, 1,030°C, 1 sec)

FIG. 27B



$CoSi_2$ FORMATION

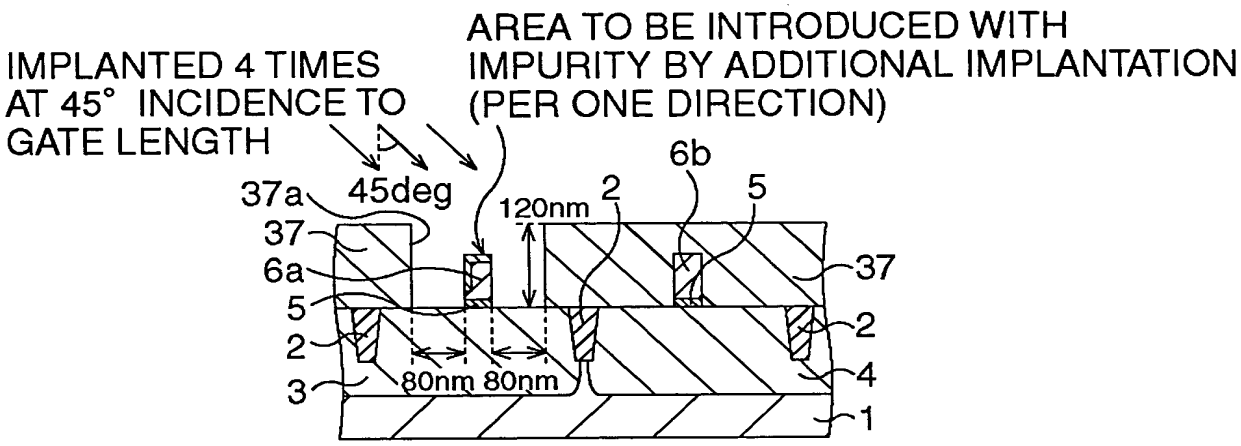
FIG. 27C



METALLIZATION

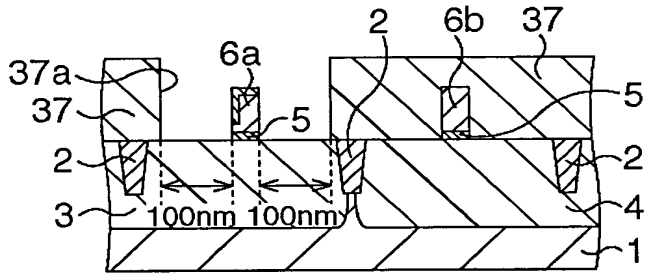
FIG. 28A

TRIMMED RESIST PREVENTS POCKET FROM BEING HIDDEN THEREWITH, AND MODERATES RESTRICTION ON ANGLE OF INCIDENCE OF POCKET IMPLANTATION.



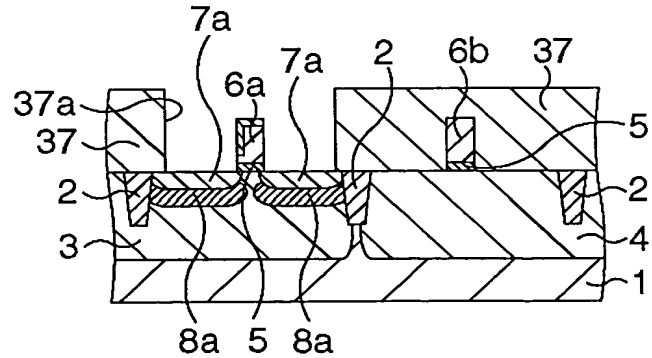
nMOS GATE IMPLANTATION (P, 4 keV, $5 \times 10^{14} \times 4$, 45°)

FIG. 28B



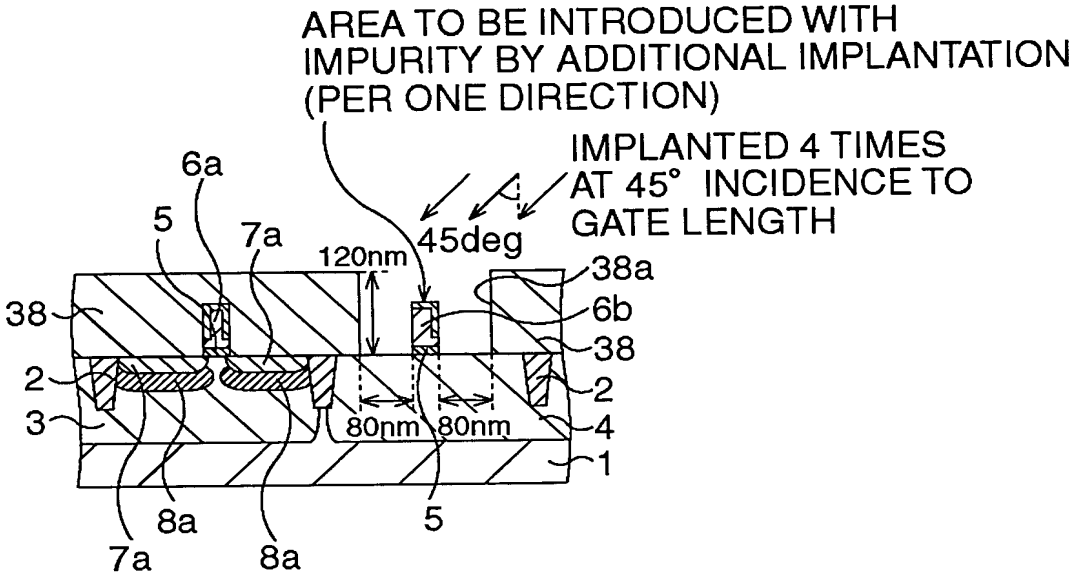
RESIST TRIMMING (20 nm)

FIG. 28C



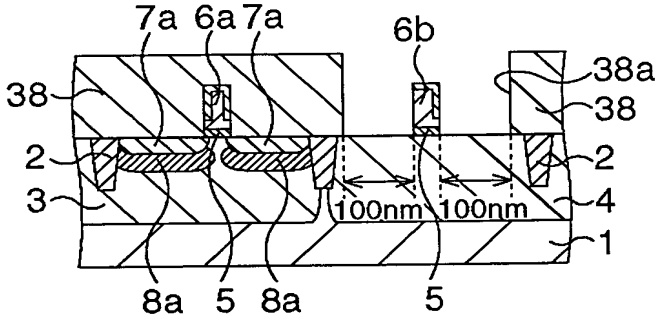
nMOS EXTENSION IMPLANTATION (0°)
AND POCKET IMPLANTATION (30°)

FIG. 29A



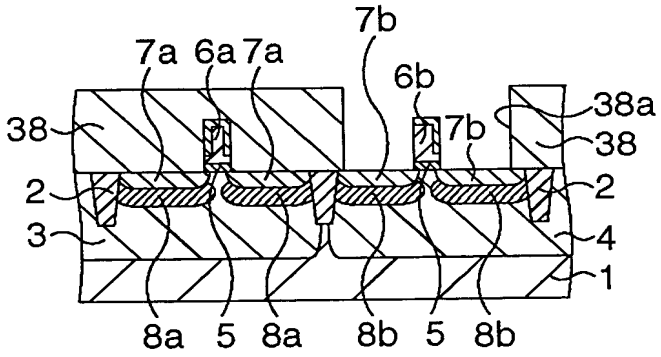
pMOS GATE IMPLANTATION (B, 2 keV, $2.5 \times 10^{14} \times 4$, 45°)

FIG. 29B



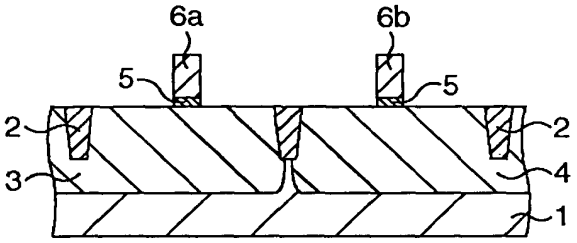
RESIST TRIMMING (20 nm)

FIG. 29C



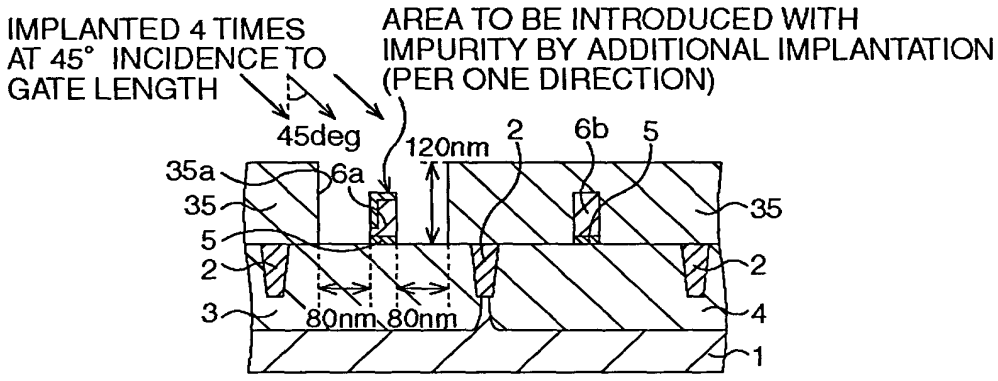
pMOS EXTENSION IMPLANTATION (0°)
AND POCKET IMPLANTATION (30°)

FIG. 30A



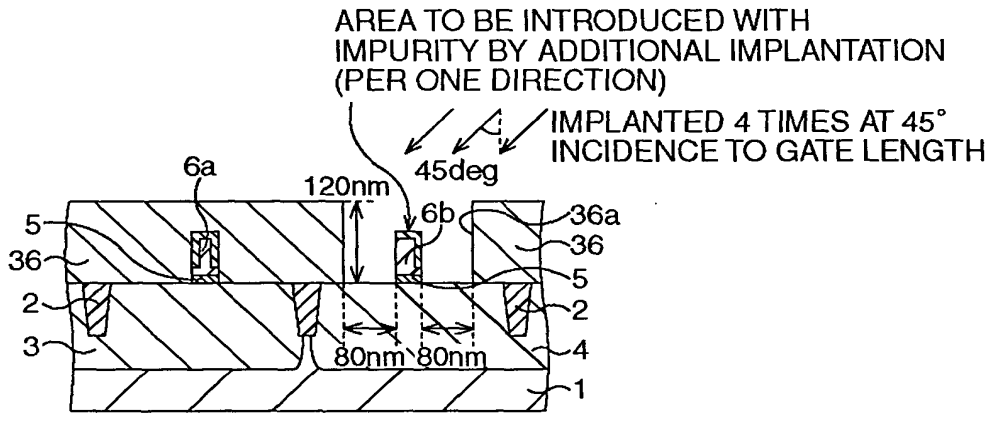
POLYSILICON ETCHING

FIG. 30B



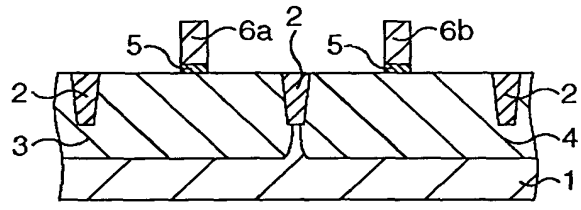
nMOS GATE IMPLANTATION (P, 4 keV, $5 \times 10^{14} \times 4$, 45°)

FIG. 30C



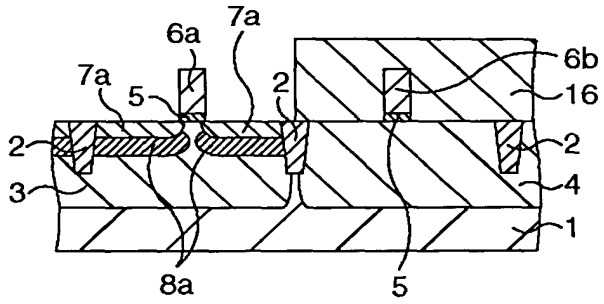
pMOS GATE IMPLANTATION (B, 2 keV, $2.5 \times 10^{14} \times 4$, 45°)

FIG. 30D



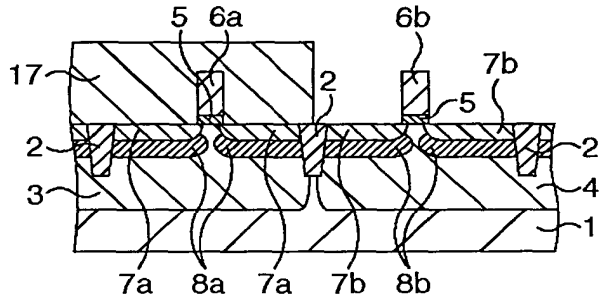
ANNEALING (RTA, 1,050°C, 1 sec)

FIG. 31A



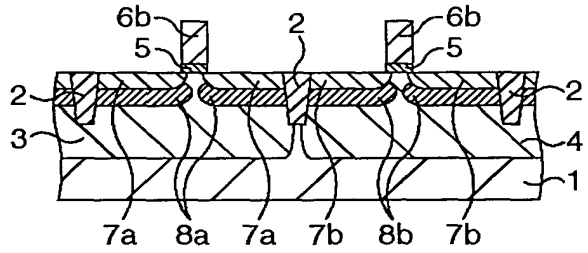
nMOS EXTENSION AND POCKET ION IMPLANTATIONS

FIG. 31B



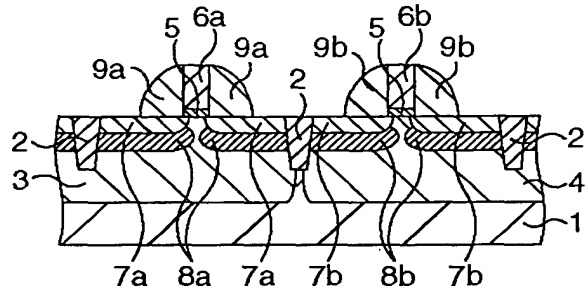
pMOS EXTENSION AND POCKET ION IMPLANTATIONS

FIG. 31C



ANNEALING (RTA, 1,000°C, 1 sec)

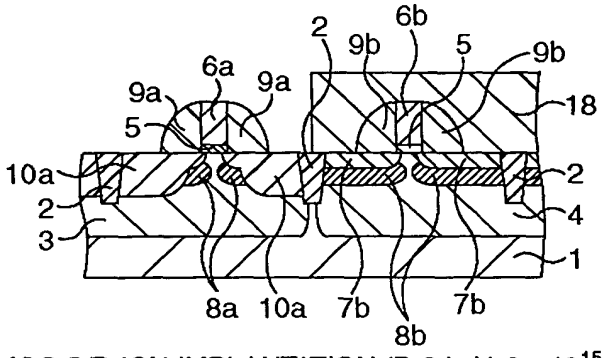
FIG. 31D



SIDEWALL FORMATION

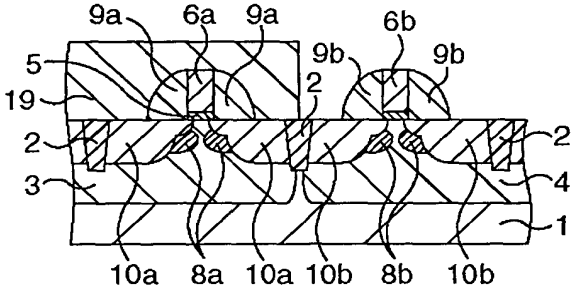
FIG. 32A

THE EIGHTH EMBODIMENT CAN LOWER THE ANNEALING TEMPERATURE AT THE STEP OF FIG. 32C THAN IN THE SIXTH EMBODIMENT SINCE THE SUBSTRATE IS ONCE ANNEALED IN THE STEP OF FIG. 30D, WHICH CAN SUPPRESS POCKET DIFFUSION AND SHORT-CHANNEL EFFECT.



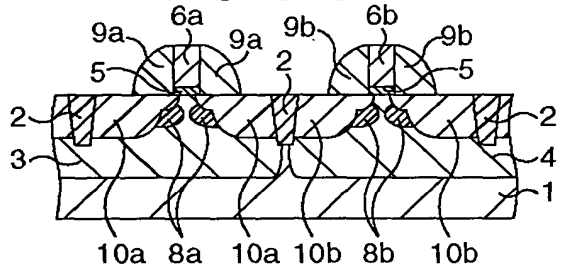
nMOS S/D ION IMPLANTATION (P, 8 keV, 6×10^{15}, 0°)

FIG. 32B



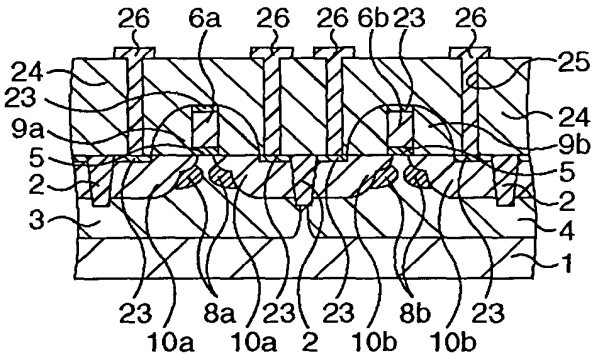
pMOS S/D ION IMPLANTATION (B, 4 keV, 3×10^{15}, 0°)

FIG. 32C



ANNEALING (RTA, 1,020°C, 1 sec)

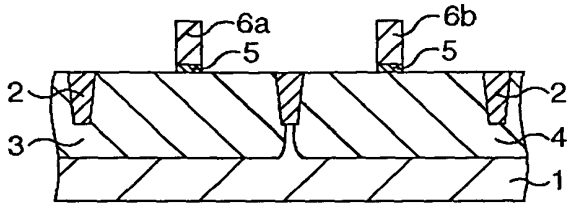
FIG. 32D



$CoSi_2$ FORMATION, METALLIZATION

FIG. 33A

THE SIXTH EMBODIMENT APPLIED TO SINGLE-DRAIN STRUCTURE.
AN ADVANTAGE RESIDES IN A LESS NUMBER OF PROCESS STEPS.

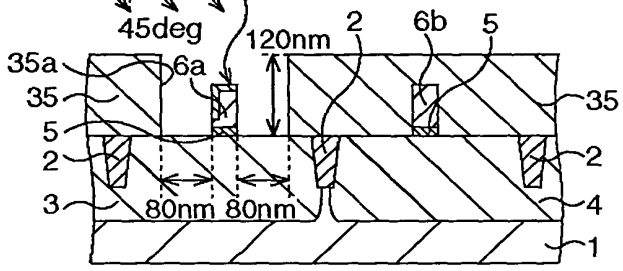


POLYSILICON ETCHING

FIG. 33B

IMPLANTED 4 TIMES
AT 45° INCIDENCE TO
GATE LENGTH

AREA TO BE INTRODUCED WITH IMPURITY BY
ADDITIONAL IMPLANTATION (PER ONE DIRECTION)

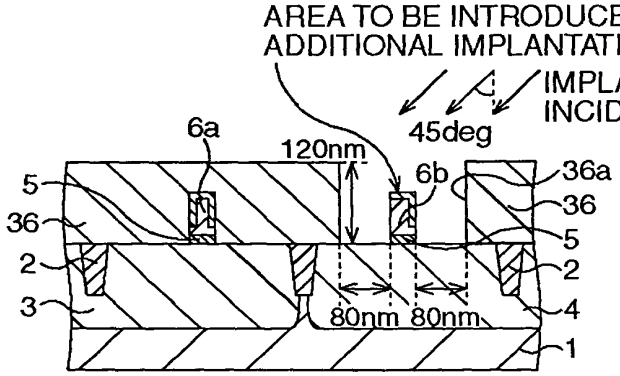


nMOS GATE IMPLANTATION (P, 4 keV, $5 \times 10^{14} \times 4$, 45°)

FIG. 33C

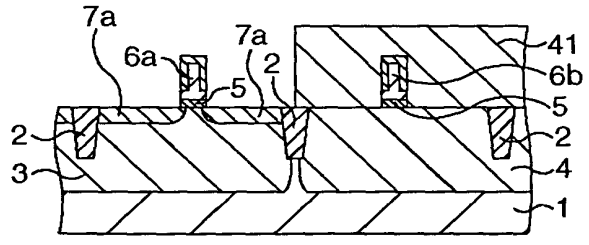
AREA TO BE INTRODUCED WITH IMPURITY BY
ADDITIONAL IMPLANTATION (PER ONE DIRECTION)

IMPLANTED 4 TIMES AT 45°
INCIDENCE TO GATE LENGTH



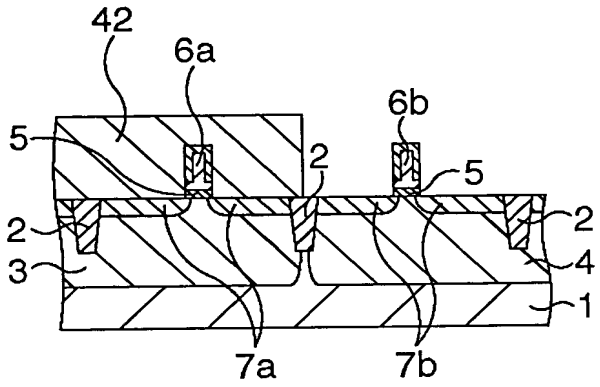
pMOS GATE IMPLANTATION (B, 2 keV, $2.5 \times 10^{14} \times 4$, 45°)

FIG. 33D



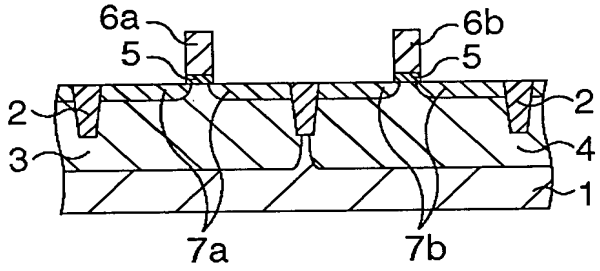
nMOS S/D ION IMPLANTATION

FIG. 34A



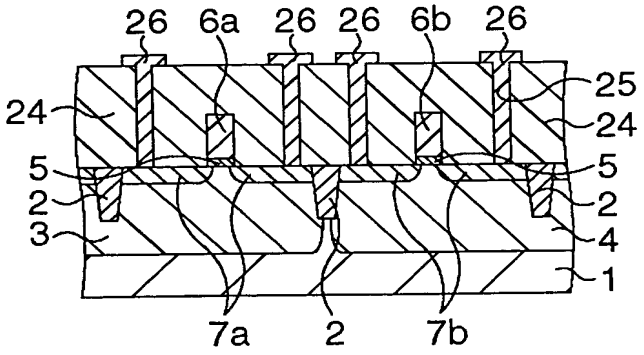
pMOS S/D ION IMPLANTATION

FIG. 34B



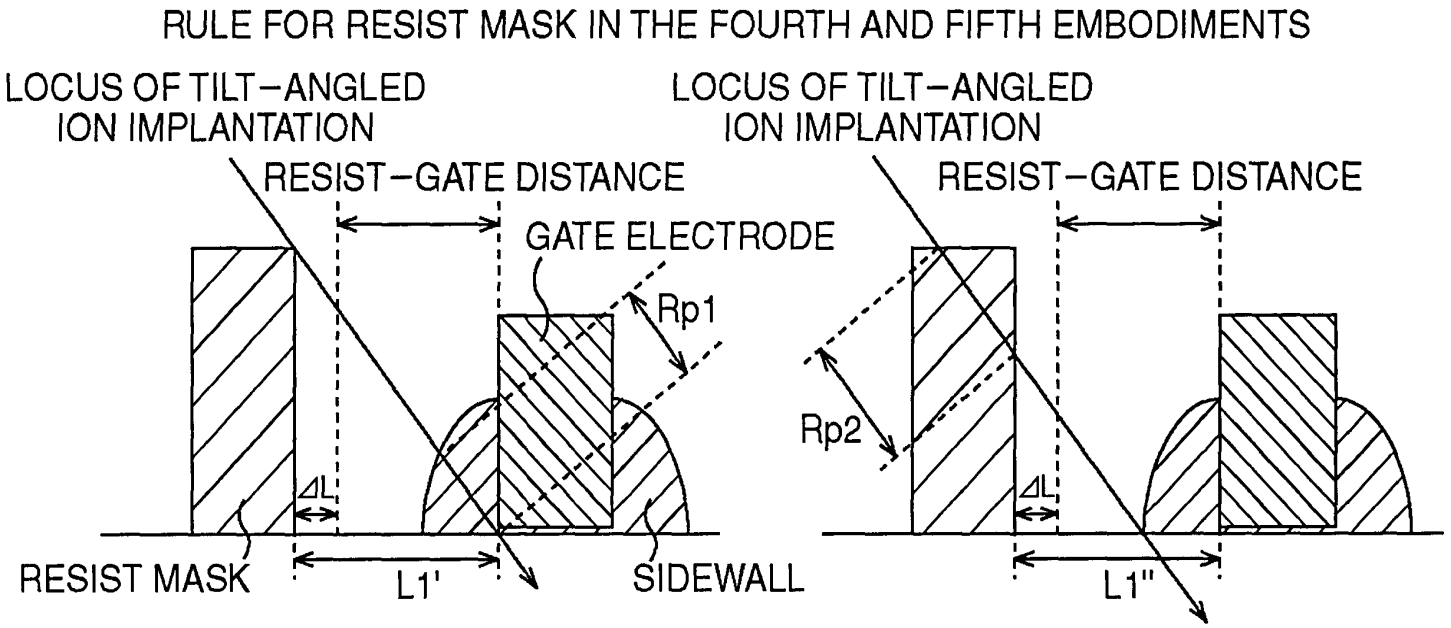
ANNEALING (RTA, 1,030°C, 1 sec)

FIG. 34C



METALLIZATION

FIG. 35



Rp1:LENGTH OF SIDEWALL SUFFICIENT FOR SHIELDING IMPURITY IMPLANTED ALONG A DIRECTION INCLINED

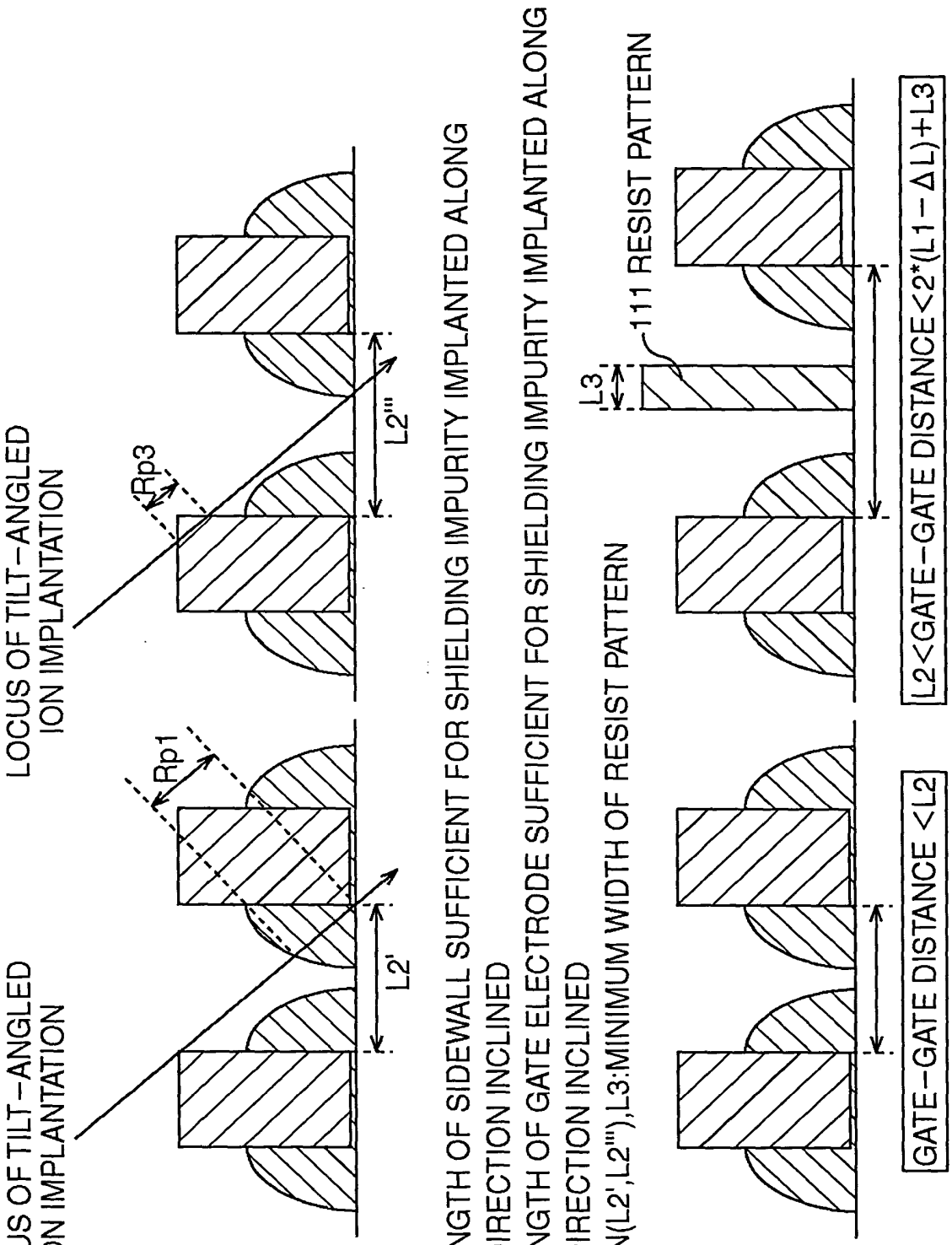
Rp2:LENGTH OF RESIST MASK SUFFICIENT FOR SHIELDING IMPURITY IMPLANTED ALONG A DIRECTION INCLINED

ΔL:ALIGNMENT ERROR BETWEEN GATE ELECTRODE AND RESIST PATTERN

L1=MIN(L1',L1")

RESIST-GATE DISTANCE=L1-ΔL

FIG. 36



Rp1:LENGTH OF SIDEWALL SUFFICIENT FOR SHIELDING IMPURITY IMPLANTED ALONG A DIRECTION INCLINED

Rp3:LENGTH OF GATE ELECTRODE SUFFICIENT FOR SHIELDING IMPURITY IMPLANTED ALONG A DIRECTION INCLINED

L2=MIN(L2',L2'''),L3:MINIMUM WIDTH OF RESIST PATTERN

FIG. 37

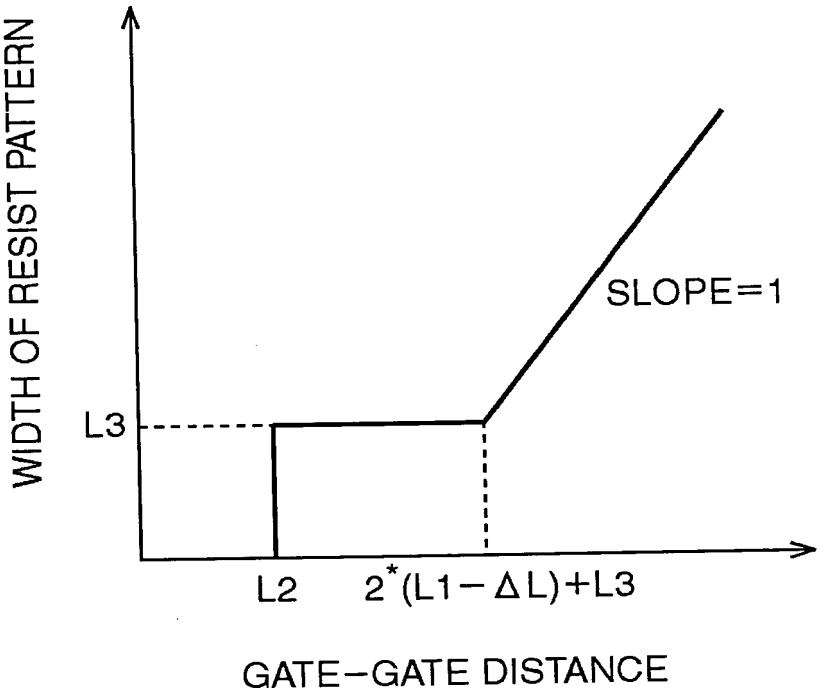
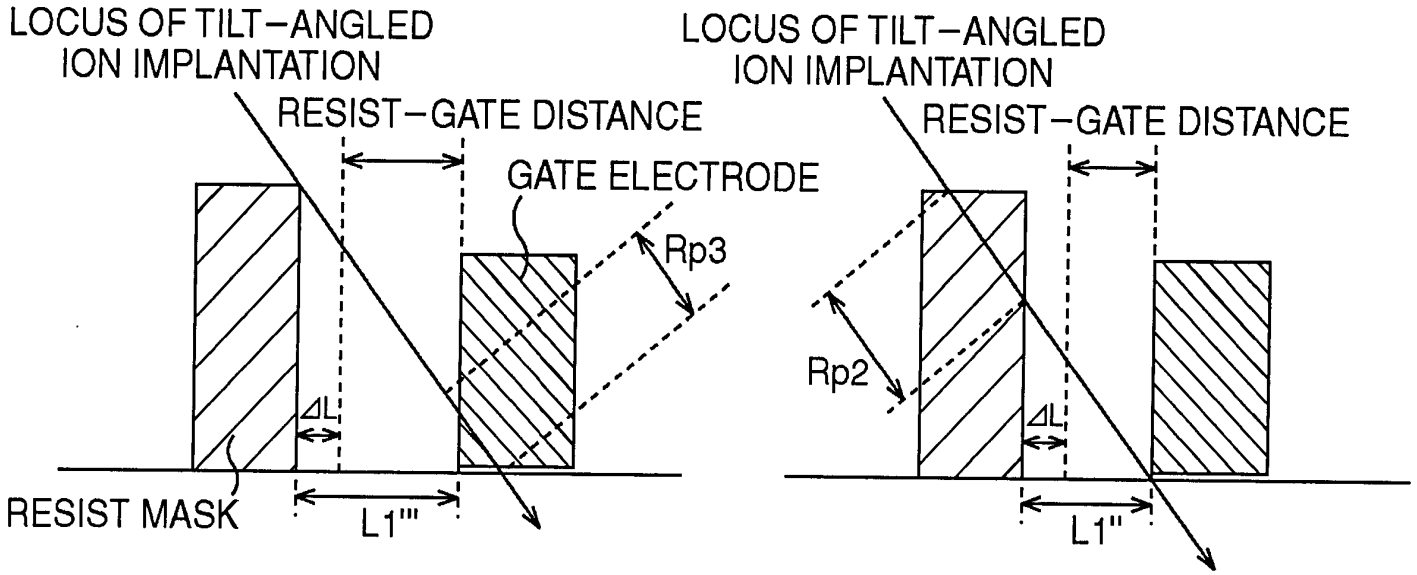

WIDTH OF RESIST PATTERN
L3
SLOPE=1
L2
2*(L1−ΔL)+L3
GATE−GATE DISTANCE

FIG. 38

RULE FOR RESIST MASK IN THE SIXTH AND EIGHTH EMBODIMENTS



Rp2:LENGTH OF RESIST MASK SUFFICIENT FOR SHIELDING IMPURITY IMPLANTED ALONG A DIRECTION INCLINED

Rp3:LENGTH OF GATE ELECTRODE SUFFICIENT FOR SHIELDING IMPURITY IMPLANTED ALONG A DIRECTION INCLINED

ΔL:ALIGNMENT ERROR BETWEEN GATE ELECTRODE AND RESIST PATTERN

L1=MIN(L1'',L1''')

RESIST-GATE DISTANCE=L1-ΔL

FIG. 39

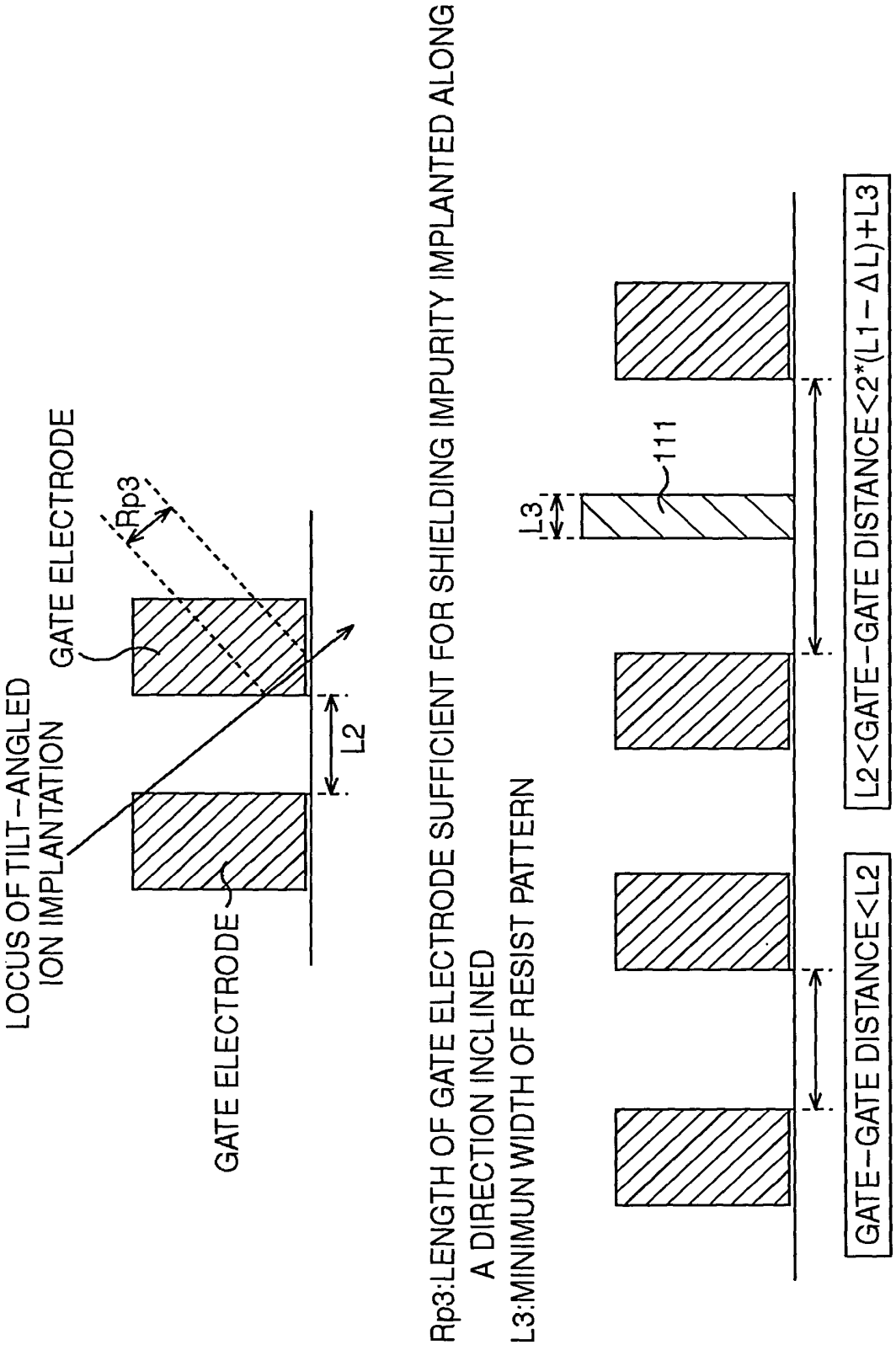

LOCUS OF TILT-ANGLED ION IMPLANTATION
GATE ELECTRODE
Rp3
L2
GATE ELECTRODE
Rp3:LENGTH OF GATE ELECTRODE SUFFICIENT FOR SHIELDING IMPURITY IMPLANTED ALONG A DIRECTION INCLINED
L3:MINIMUN WIDTH OF RESIST PATTERN
L3
111
L2<GATE-GATE DISTANCE<2*(L1-ΔL)+L3
GATE-GATE DISTANCE<L2

FIG. 40

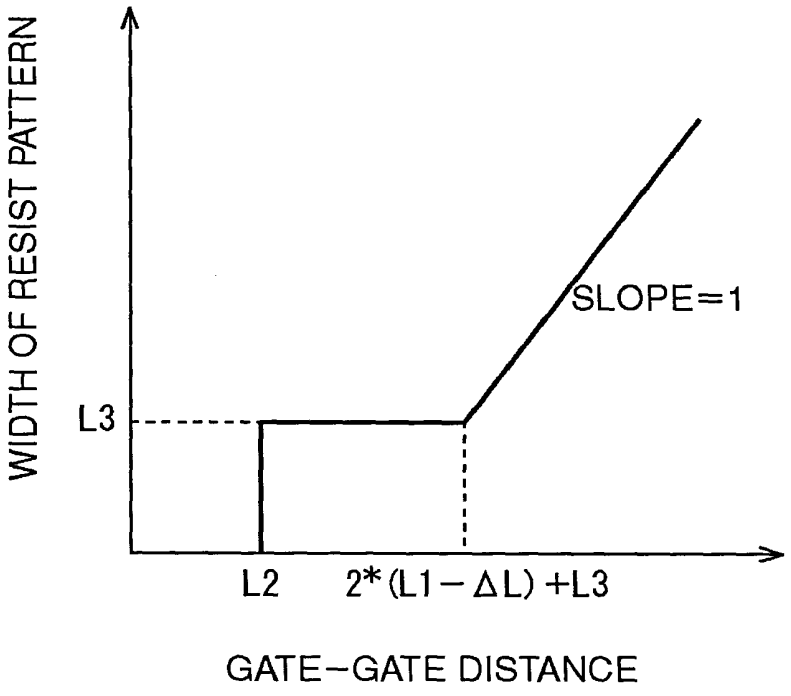
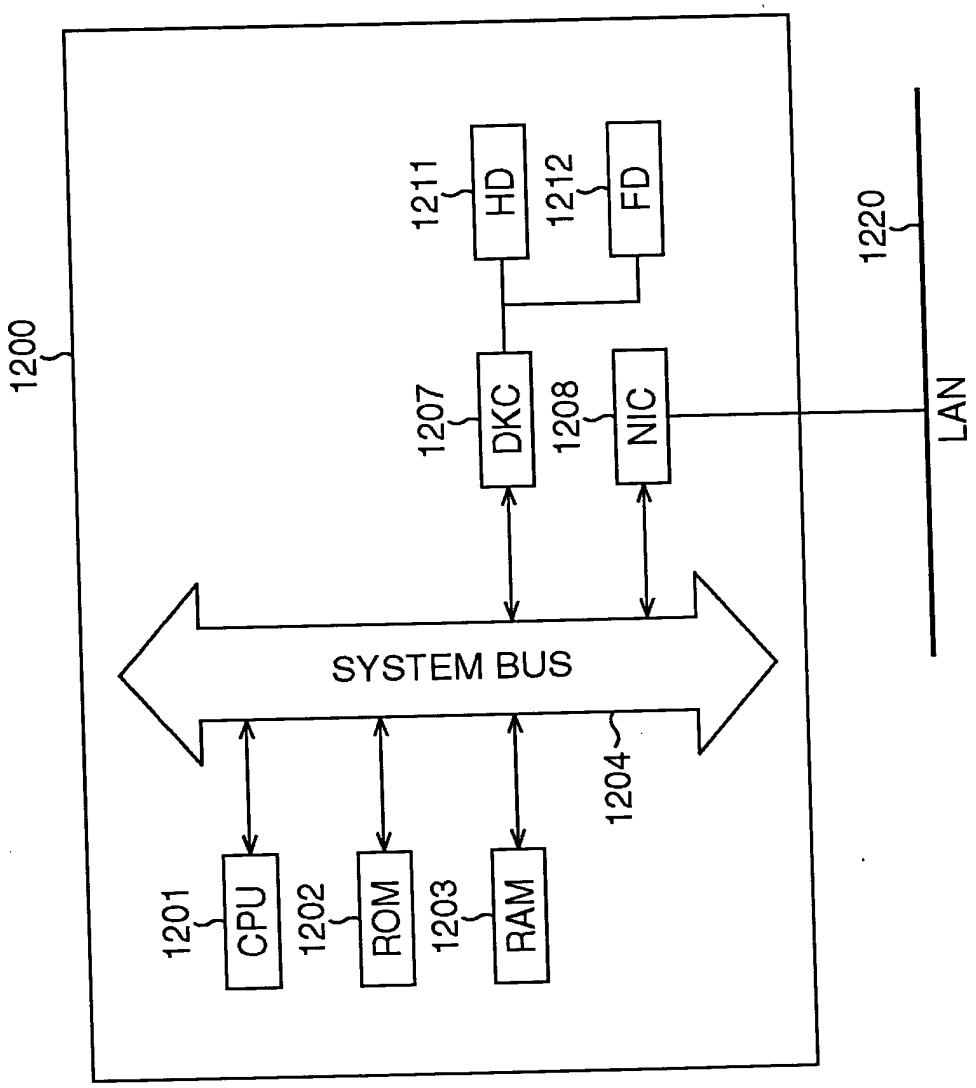

WIDTH OF RESIST PATTERN
L3
SLOPE=1
L2
2*(L1−ΔL)+L3
GATE−GATE DISTANCE

FIG. 41


1200
1211
HD
1212
FD
1220
1207
DKC
1208
NIC
LAN
SYSTEM BUS
1204
1201
CPU
1202
ROM
1203
RAM